DEPARTMENT OF ELECTRONICS ENGINEERING

Programme: UG - B.Tech

Electronics Devices and Circuits Lab (ECC210)

Laboratory Manual

INDIAN INSTITUTE OF TECHNOLOGY(ISM), DHANBAD
JHARKHAND - 826004

LIST OF EXPERIMENTS

EXPERIMENT -01

DESIGN OF OPAMP BASED CIRCUIT FOR PERFORMING VARIOUS MATHEMATICAL OPERATION (PART I).

OBJECTIVE:

After completion of this experiment, student will be able to design and setup an inverting amplifier, non- inverting amplifier and voltage follower/ buffer using OP- AMP.

APPARATUS AND COMPONENTS REQUIRED:

1. Dual power supply +/- 15V
2. DC power source
3. Function generator (0-1MHz)
4. Oscilloscope
5. Bread board (For Hardware) / Multisim Software (Software)
6. IC 741C
7. Resistor
8. Probes and connecting wires

THEORY AND EXPLANATION:

1. **INVERTING AMPLIFIER**

An inverting amplifier using op-amp is a type of amplifier where the output waveform will be 180˚ out of phase to the input waveform. The input waveform will be amplified by the factor A_v (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit, the signal to be amplified is applied to the inverting input of the op-amp through the input resistance R_1. R_f is the feedback resistor. R_f and R_1 together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation $A_F = -R_F/R_1$. Negative sign implies that the output signal is out of phase.

At the node v_2, we have $i_{in} = i_F + i_{B2}$. Since R_i is very large, the bias current is negligibly small and we can write $i_{in} \cong i_F$

Or, $\frac{v_{in} - v_2}{R_1} = \frac{v_2 - v_o}{R_F}$.

Again, $v_1 - v_2 = v_o/A$.

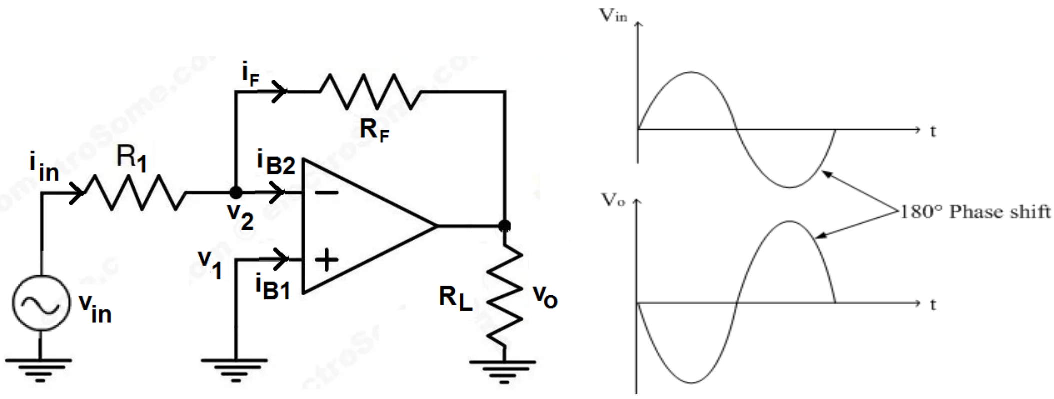
Since $v_1 = 0$, we get $v_2 = -v_o/A$.

Therefore,

$$\frac{v_{in} + (v_o/A)}{R_1} = \frac{-(v_o/A) - v_o}{R_F}$$

Or, $$A_F = \frac{v_o}{v_{in}} = -\frac{AR_F}{R_1 + R_F + AR_1}$$

Since the internal gain of the OPAMP (A) is very high we can assume $AR_1 \gg R_1 + R_F$ and $A_F = -R_F/R_1$. The negative sign indicates that the input and output signals are 180^o out of phase. Further if $R_1 = R_F$ the output signal is equal in amplitude but opposite in phase to that of input signal. This circuit represents an inverter.



(a) (b)

Fig.1.1. (a) Circuit diagram, (b) Input and output Waveform of inverting amplifier

This means that if we replace the v_{in} and R_1 combination by a current source i_{in}, as shown Fig. 1.2, the output voltage v_o becomes proportional to the input voltage. In other words the figure represents a current to voltage converter that converts the input current into a proportional output voltage.

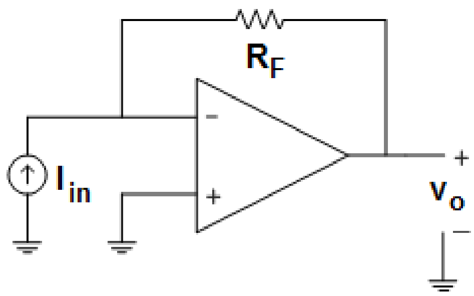
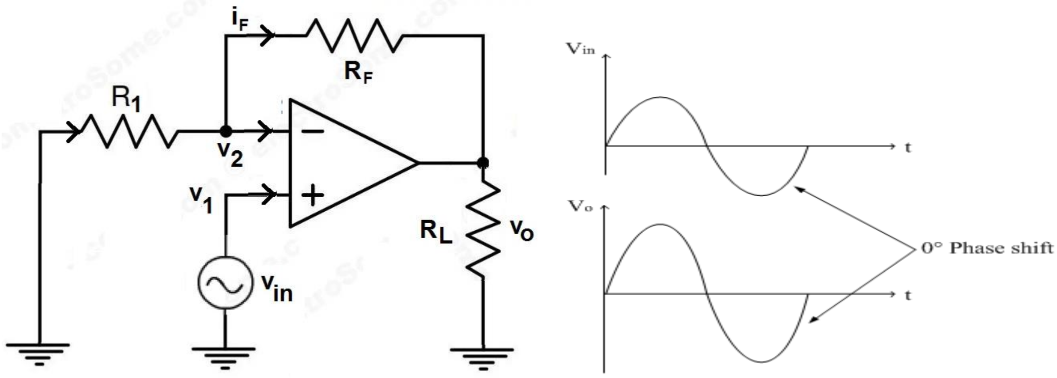


Fig. 1.2 Current to Voltage Converter

II. NON- INVERTING AMPLIFIER

A non-inverting amplifier is an op-amp circuit configuration which produces an amplified output signal is shown in Fig 1.3. This output signal of non-inverting OPAMP is in-phase with the input signal applied.



(a) (b)

Fig.1.3. (a) Circuit diagram, (b) Input and output Waveform of non- inverting amplifier

At the input loop, $v_{id} = v_{in} - v_f$.

The closed loop gain is $A_F = v_o / v_{in}$.

Again, $v_o = A(v_1 - v_2)$.

Now, $v_1 = v_{in}$ and $v_2 = v_f = \frac{R_1}{R_1 + R_F} v_o$ (assuming $R_i \gg R_1$).

Therefore, $v_o = A\left(v_{in} - \frac{R_1 v_o}{R_1 + R_F} \right)$

Or, $v_o = \frac{A(R_1 + R_F) v_{in}}{R_1 + R_F + AR_1}$.

Thus, $A_F = \frac{v_o}{v_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1}$.

Since A is very large, we can assume $AR_1 \gg R_1 + R_F$ and therefore $A_F = 1 + \frac{R_F}{R_1}$.

If we open the resistance R_1 and short the resistance R_F, as shown in Fig. 1.4, then the gain of the non-inverting amplifier becomes lowest and equal to one. Such circuit is called a voltage follower because the output voltage is equal and in phase with the input. In other words the output follows the input. It is similar to the discrete emitter follower, but the voltage follower is preferred over emitter follower as it has much higher input resistance and the output amplitude is exactly equal to the input.

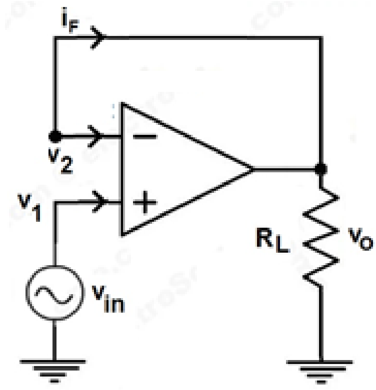


Fig. 1.4. Voltage Follower Circuit

PROCEDURE:

1. Derive / Check the component values [Typical values of resistors are in kΩ].
2. Setup the circuit on the breadboard / Multisim software and check the connections (for software simulation).
3. Apply suitable ac voltage levels and waveforms at the input terminal. [Typical values 1-2 Vpp, Frequency = 1 kHz, Waveform: Sinusoidal, dc / ac for voltage follower]
4. Observe input and output on two channels of the oscilloscope simultaneously. Note down and draw the input and output waveforms on the graph.
5. Compare the practical values with theoretical values.
6. For the frequency response of the inverting and non- inverting amplifier, vary the frequency of the input waveform and enter into the tabular column. Also plot the frequency curve.
7. For voltage follower circuit, feed a waveform to the input and note down the output amplitude by varying the input amplitude of the waveform. Enter it in the tabular column.

OBSERVATION TABLE:

TABLE - 1: FOR INVERTING / NON-INVERTING AMPLIFIER

R_1 (kΩ)	R_f(kΩ)	V_{in} (Volt)	V_o (Volt)	Theoretical Gain	Practical Gain (dB)

TABLE - 2: FOR FREQUENCY RESPONSE OF THE INVERTING / NON- INVERTING AMPLIFIER

Frequency (Hz - kHz)	V_0 (V)	Gain	Gain(dB)

TABLE - 3: FOR VOLTAGE FOLLOWER

Input	Output		Input	Output	
V_{in} (dc)	Theoretical	Practical	V_{in} (ac)	Theoretical	Practical

OBJERVATIONS:

Explain your result here.

CONCLUSION:

Various mathematical operation of OPAMP such inverting, non- inverting amplifier and voltage buffer has been studied.

PROBLEMS:

1. Design an inverting op-amp circuit for which the gain is -5V/V and the total resistance used is 120 kohm.
2. Calculate the output voltage of a non- inverting amplifier for values of V_1 = 2V, R_f = 500 kohm and R_1 = 100 kohm
3. An op-amp with an open loop gain of 100V/V is used in the inverting configuration. If in this application the output voltages range from -10V to +10V, what is the maximum voltage by which the virtual ground node departs from its ideal value.
4. What is the typical conditions of non- inverting amplifier to operate in linear region?

TYPICAL QUESTIONS:

1. In what way the voltage follower is the special case of non-inverting amplifier and current-to-voltage converter is the special case of inverting amplifier?
2. What kind of feedback is present in inverting /non- inverting amplifier?
3. What is virtual ground? What happens when the inverting / non-inverting is not grounded in case of non-inverting / inverting amplifier?
4. Describe different pin configurations of IC741C.

5. How to design an inverting / non-inverting amplifier for a specified gain?
6. How the feed-back effects the input and output resistance of an inverting / non-inverting amplifier as compared to an open loop OPAMP?
7. How the feed-back effects the gain and bandwidth of an inverting / non-inverting amplifier as compared to an open loop OPAMP?
8. What are the general assumptions that we make during the design of an OPAMP feedback circuit.
9. What are the characteristics of an ideal and a practical OPAMP?
10. Define different parameters (such as input offset voltage, input offset current, input bias current, slew rate, CMRR etc.) related to OPAMP.

EXPERIMENT -2

DESIGN OF OPAMP BASED CIRCUIT FOR PERFORMING VARIOUS MATHEMATICAL OPERATION (PART II).

OBJECTIVE:

After completion of this experiment, student will be able to design and setup a summing amplifier, difference amplifier, integrator, differentiator using OPAMP.

APPARATUS AND COMPONENTS REQUIRED:

1. Dual power supply +/- 15V
2. DC power source
3. Function generator (0-1MHz)
4. Oscilloscope
5. Bread board (For Hardware) / Multisim Software (Software)
6. IC 741C
7. Resistor
8. Capacitor
9. Probes and connecting wires

THEORY AND EXPLANATION

1. **ADDER**

OPAMP can be used to design a circuit whose output is the sum of two or more input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non-inverting summer depending on the input applied to inverting & non-inverting terminals respectively. Circuit diagram Fig.2.1 (a) shows an N-input inverting summing amplifier whereas circuit diagram 2.1 (a) shows an N-input non-inverting summing amplifier. For inverting summing amplifier the output will be amplified version of the sum of the N input voltages with 180^0 phase reversal whereas for non-inverting summing amplifier the output will be amplified version of the sum of the N input voltages with 0^0 phase difference.

N-input inverting summing amplifier:

$i_{in} = i_1 + i_2 + \cdots i_N \cong i_F$

Or, $\dfrac{v_1 - 0}{R_1} + \dfrac{v_2 - 0}{R_2} + \cdots + \dfrac{v_N - 0}{R_N} = \dfrac{0 - v_0}{R_F}$.

Or, $\dfrac{v_1}{R_1} + \dfrac{v_2}{R_2} + \cdots + \dfrac{v_N}{R_N} = -\dfrac{v_0}{R_F}$

Or, $v_0 = -R_F\left(\dfrac{v_1}{R_1} + \dfrac{v_2}{R_2} + \cdots + \dfrac{v_N}{R_N}\right)$

Such amplifier is called scaling or weighted amplifier as each input voltage is amplified by a different factor. If $R_1 = R_2 = \cdots = R_N = R$ then $v_0 = -R_F\left(v_1 + v_2 + \cdots + v_N\right)/R$ .If $R_F/R = 1/N$ then $v_0 = -\left(v_1 + v_2 + \cdots + v_N\right)/N$. Therefore the output is the average of the input voltages. Further if $R_F = R$ then $v_0 = -\left(v_1 + v_2 + \cdots + v_N\right)$. Thus output is the algebraic sum of the input voltages.

N-input non-inverting summing amplifier:

Using superposition principle at node V_1 we can write

$$V_1 = \frac{R/2}{R + R/2}V_a + \frac{R/2}{R + R/2}V_b + \frac{R/2}{R + R/2}V_c$$

Or, $V_1 = \left(V_a + V_b + V_c\right)/3$

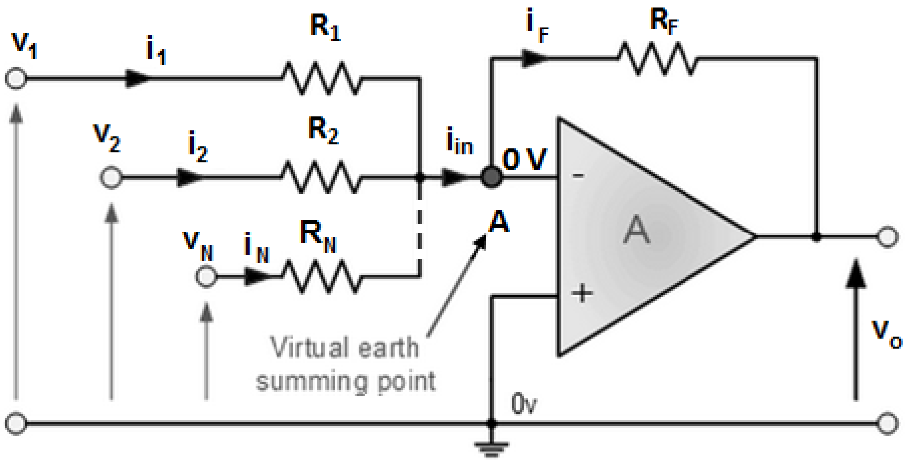
Now, $\dfrac{0 - V_2}{R_1} = \dfrac{V_2 - V_o}{R_F}$

Or, $\dfrac{V_o}{R_F} = \dfrac{V_2}{R_F} + \dfrac{V_2}{R_1} = V_2\left(\dfrac{R_1 + R_F}{R_1 R_F}\right)$

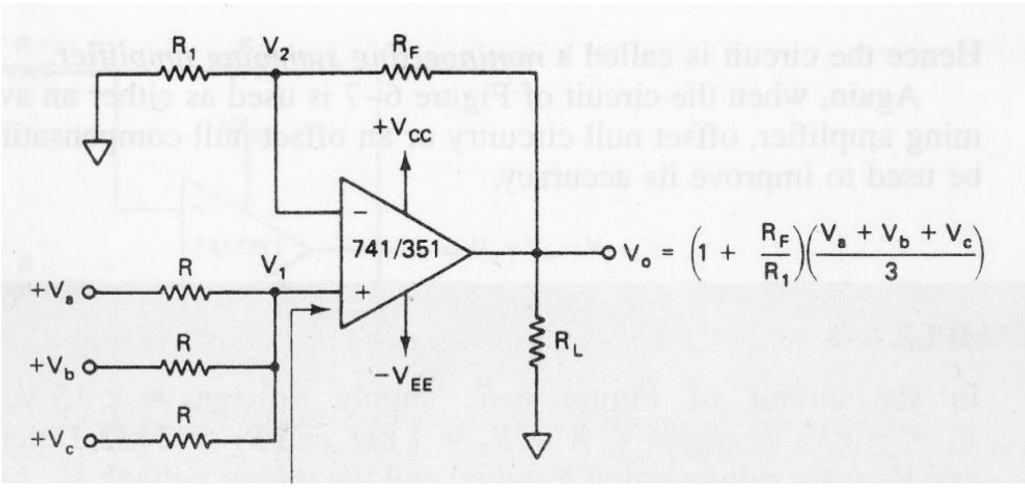
Or, $V_o = V_2\left(\dfrac{R_1 + R_F}{R_1}\right) = V_2\left(1 + \dfrac{R_F}{R_1}\right)$

Since $V_2 = V_1$ we can write, $V_o = \left(1 + \dfrac{R_F}{R_1}\right)\dfrac{V_a + V_b + V_c}{3}$.

Above equation implies that output voltage is average of the input voltage times the gain of the circuit $1 + \dfrac{R_F}{R_1}$. Such amplifier is known as averaging amplifier. To get the actual average R_F should be zero and R_1 should be opened. To get summed output $1 + \dfrac{R_F}{R_1}$ should be equal to 3 or R_F should be equal to $2R_1$.



(a)



(b)

Fig.2.1. Circuit diagram of adder (a) Inverting summing amplifier, (b) Non-inverting summing amplifier

2. SUBTRACTOR

A difference or subtractor amplifier is a circuit that gives the amplified version of the difference of the two inputs. An OPAMP differential amplifier is shown in circuit diagram Fig.2.2.

At node v_x we can write, $\frac{v_1 - v_x}{R_1} = \frac{v_x - v_o}{R_2}$

Since $v_x = v_y$ at node v_y we can write, $\frac{v_2 - v_x}{R_1} = \frac{v_x - 0}{R_2}$.

Subtracting the former equation from the later, we get $\frac{v_2 - v_x - v_1 + v_x}{R_1} = \frac{v_x - v_x + v_o}{R_2}$

Or, $v_o = R_2(v_2 - v_1)/R_1$.

Above equation implies that output voltage is difference of the input voltage times the gain of the circuit R_2/R_1 . Such amplifier is known as difference amplifier.

To get actual difference output (or subtraction) R_2/R_1 should be equal to 1 or R_2 should be equal to R_1.

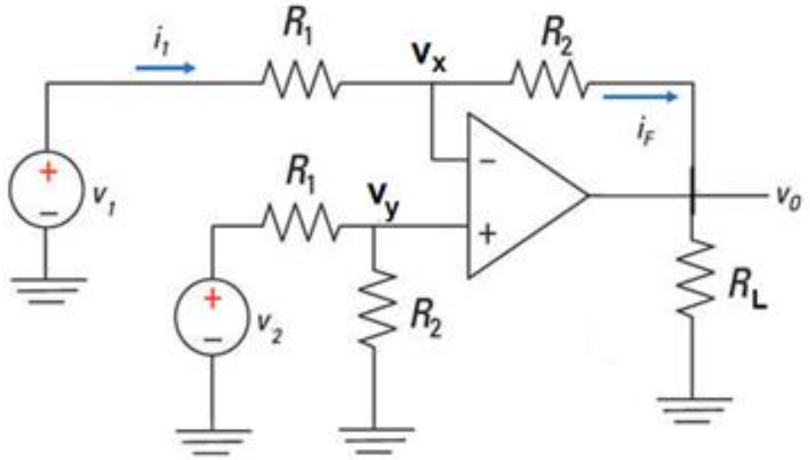


Fig.2.2. Circuit diagram for subtractor.

3. INTEGRATOR

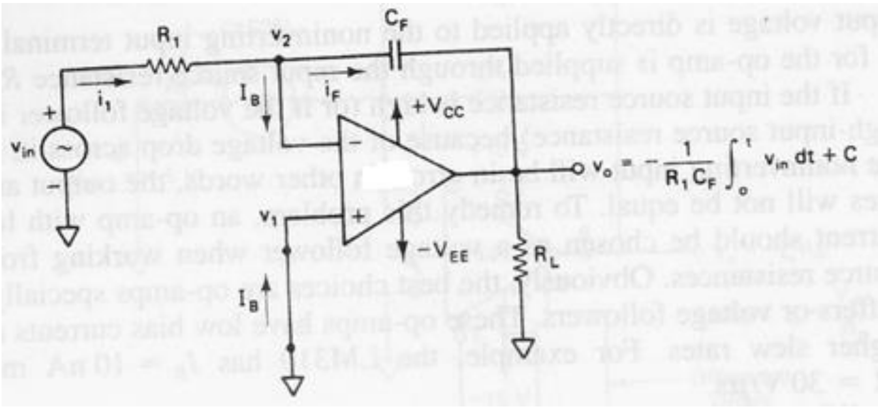
It is a closed loop op-amp circuit which performs the mathematical operation of integration. That is the output waveform is the integral of the input voltage. This circuit also works as low pass filter. The integrator circuit is constructed from basic inverting amplifier by replacing the feedback resistance with a capacitor, as shown in circuit diagram 2.3. Since the non-inverting terminal is at ground potential we can assume the node v_2 is at ground potential.

From the circuit we can write $\frac{v_{in} - 0}{R_1} = C_F \frac{d}{dt}(0 - v_o)$

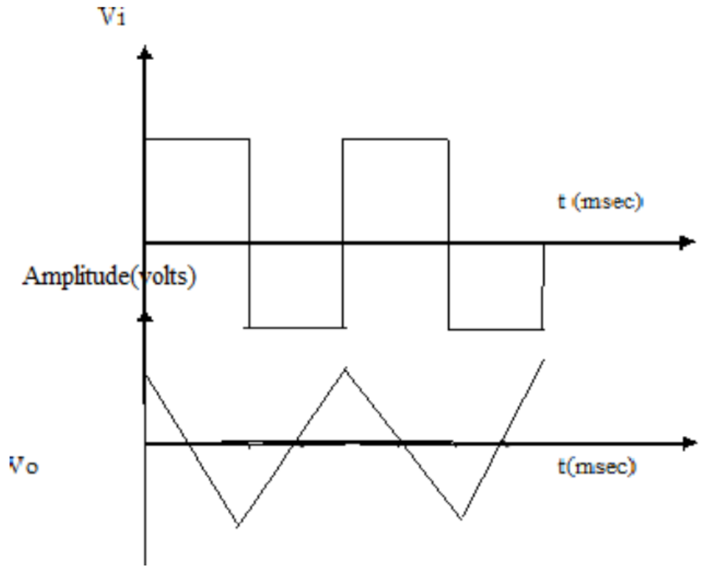
Or, $\frac{v_{in}}{R_1} = -C_F \frac{dv_o}{dt}$.

Or, $v_o = -\frac{1}{R_1 C_F} \int_0^t v_{in} dt + C$

where "C" is the integration constant and is proportional to the value of output voltage v_o at time t = 0.



(a)



(b)

Fig.2.4. (a) Circuit diagram for integrator and (b) its input and output waveform

When $v_{in} = 0$ the integrator works as an open-loop amplifier, because the capacitor acts as an open circuit to the input offset voltage V_{io}.Therefore a practical integrator uses a resistor R_F across C_F, as shown in circuit diagram 2.4.The R_F limits the low frequency gain and hence minimizes the variations in the output voltage.

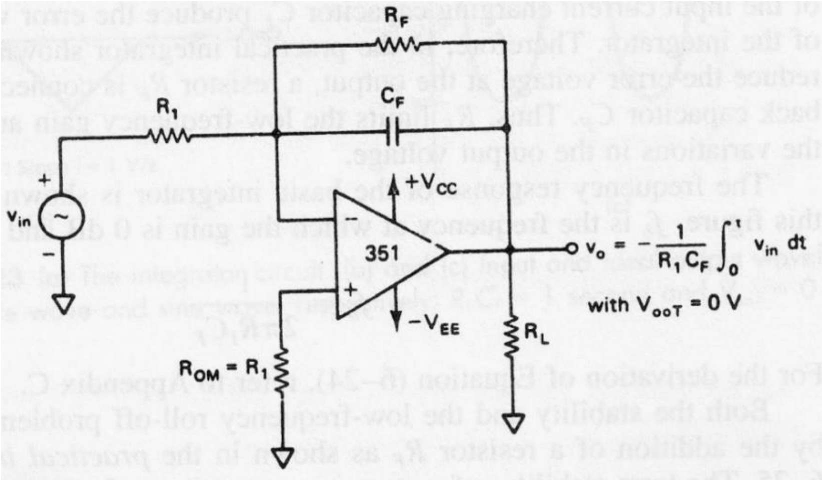


Fig. 2.4. Practical integrator

5. DIFFERENTIATOR

It is an OPAMP circuit which performs the mathematical operation of differentiation. That is the output waveform is the derivative or differential of the input voltage. This circuit also works as high pass filter.The differentiator circuit is constructed from basic inverting amplifier by replacing the input resistance with a capacitor, as shown in circuit diagram 2.5.Since the non-inverting terminal is at ground potential we can assume the node v_2 is at ground potential.

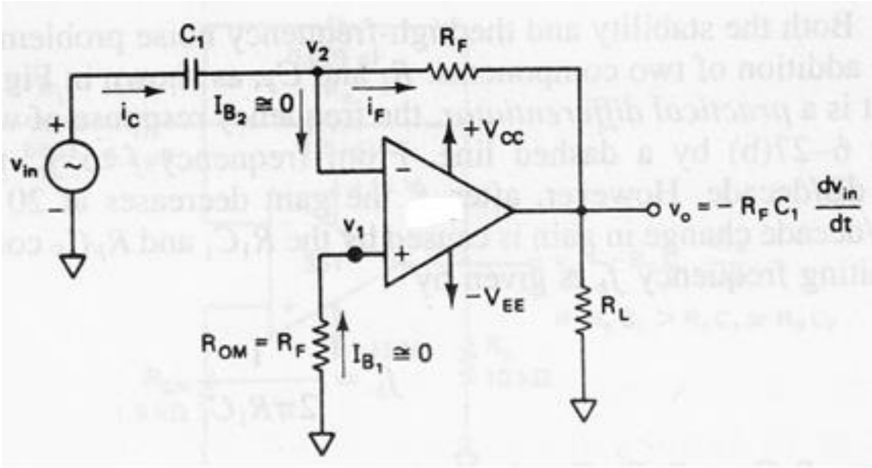
From the circuit we can write

$$C_1 \frac{d}{dt}\left(v_{in} - 0\right) = \frac{0 - v_o}{R_F}$$

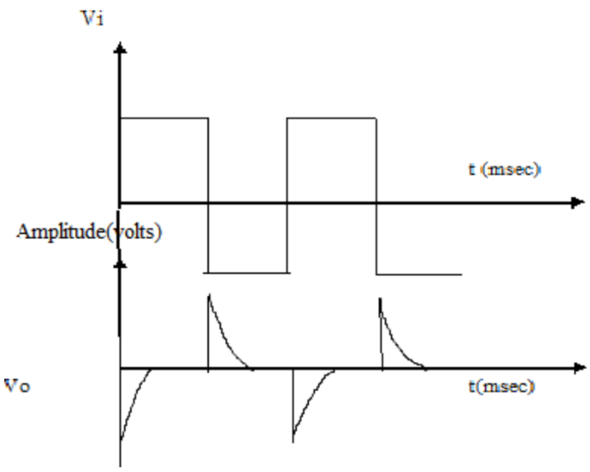
Or, $v_o = -R_F C_1 \dfrac{dv_{in}}{dt}$.

Above equation implies the output voltage is $C_F R_1$ times the negative instantaneous rate of change of v_{in} with time. Therefore a cosine input will produce a sine wave output, or a triangular input will produce a square wave output

When v_{in} = 0 the differentiator works as an open-loop amplifier, because the capacitor acts as an open circuit to the input offset voltage V_{io}.Therefore a practical differentiator uses a series resistor with the capacitor.



(a)



(b)

Fig.2.5. (a) Circuit diagram for differentiator and (b) its input and output waveform.

PROCEDURE:

1. Derive / Check the component values [Typical values of resistors are in kΩ and capacitors in µF. The feedback resistor in circuit diagram 2.4 should be very high as compared to other resistors].
2. Setup the circuit on the breadboard / Multisim software and check the connections (for software simulation).
3. Apply suitable voltage levels and waveforms (DC + DC /DC + ac /ac + ac / ac) at the input terminal(s). [Typical values DC: 1 – 2 V, ac: 1-2 V pp, Frequency = 1 kHz, Waveform: Sinusoidal for adder and subtractor, square wave for integrator and differentiator]
4. Observe input and output on two channels of the oscilloscope simultaneously. Note down and draw the input and output waveforms on the graph.
5. Compare the practical values with theoretical values.

6. For integrator / differentiator feed a waveform to the input and note down the output amplitude by varying the frequency of the waveform. Enter it in the tabular column and plot the frequency curve. [Typical waveform: square wave, Frequency: From few Hz to few kHz]

OBSERVATION TABLE:

TABLE -1: FOR ADDER / SUBTRACTOR CIRCUIT

Input		Output		Input		Output		Input		output	
V1(dc)	V2(dc)	Theoretical	Practical	V1(dc)	V2(ac)	Theoretical	Practical	V1(ac)	V2(ac)	Theoretical	Practical

TABLE- 2: FOR INTEGRATOR/ DIFFERENTIATOR

Type	Input waveform	Output waveform	Output voltage(theoretical)	Output voltage(practical)	% error
Differentiator /Integrator					

TABLE- 3: FOR INTEGRATOR/ DIFFERENTIATON

Frequency	V_{in} (Volt)	V_o (Volt)	Gain (dB)

OBSERVATIONS:

Explain your result here.

CONCLUSION:

Various mathematical operation of OPAMP such as adder, subtractor, integrator and differentiator has been studied. The realization of differentiation act as high pass filter and integration act as low pass filter also has been studied.

PROBLEMS:

1. Design a circuit using OPAMP to add 3/4 numbers.
2. Design a circuit using OPAMP to perform 5 - 3 = 2
3. Design a circuit using OPAMP to perform integration of a square wave of PRF 1 KHz
4. Design a circuit using OPAMP to perform differentiation of a square wave of PRF 1 KHz/2 KHz/3KHz

TYPICAL QUESTIONS:

1. What happens to the accuracy of integration as the input frequency is increased?
2. At very low frequencies, does the integrator behave more like a true integrator, or like an amplifier?
3. What is the purpose of the feedback resistor in circuit diagram 2.4?
4. What happens to the accuracy of differentiation as the input frequency is decreased?
5. At very high frequencies, does the differentiator behave more like a true differentiator, or like an amplifier?
6. What is the purpose of the series resistor in circuit diagram 2.5?
7. How can you design an average amplifier?
8. What are the general assumptions that we make during the design of an OPAMP feedback circuit.
9. What are the characteristics of an ideal and a practical OPAMP?
10. Define different parameters (such as input offset voltage, input offset current, input bias current, slew rate, CMRR etc.) related to OPAMP.

OTHER RELATED OPAMP CIRCUIT DESIGN:

1. Summing amplifier using differential configuration
2. Instrumentation amplifier
3. Differential input and differential output amplifier
4. Voltage to current converter
5. Logarithmic Amplifier
6. Anti-logarithmic amplifier.

EXPERIMENT -03

DESIGN AND PERFORMANCE ANALYSIS OF VARIOUS ACTIVE FILTERS.

OBJECTIVE:

After completion of this experiment, student will be able to design 1^{st} order and 2^{nd} order low pass filter and high pass filter by using Op-Amp.

APPARATUS AND COMPONENTS REQUIRED:

1. Dual power supply +/- 15V
2. DC power source
3. Function generator
4. Oscilloscope
5. Bread board (For Hardware) / Multisim Software (Software)
6. IC 741C
7. Resistor (Order: kΩ)
8. Capacitors (Order: µF)
9. Probes and connecting wires

THEORY AND EXPLANATION:

1. **LOW PASS FILTER**

It is a network that allows the flow of signal with frequency below the cut-off frequency, f_H, and blocks the signals with frequency above the cut-off frequency. Here, few active low pass filters are realized by using Op-amp. Active low pass filters have the same principle of operation and frequency response as passive low pass filter, the only difference is that it uses an op-amp for amplification and gain control. The simplest form of an active low pass filter is a passive low pass filter connected at the input of an inverting /non-inverting amplifier.

First-order low-pass Butterworth filter:

Schematic diagram of a first –order low-pass Butterworth filter is shown below.

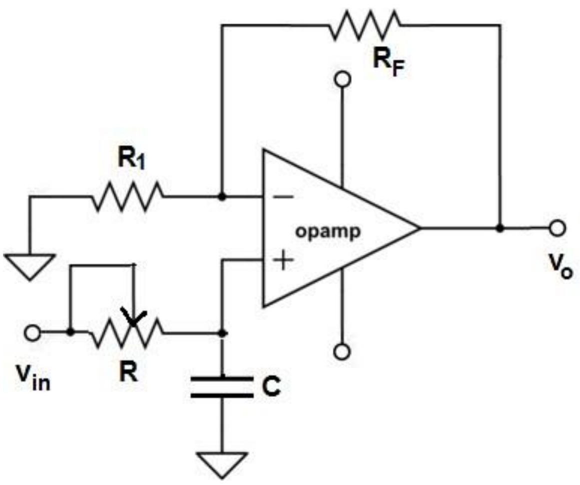


Fig. 3.1. Circuit diagram of a First-order low-pass filter.

The OPAMP is used in the non-inverting condition; hence it does not load down the RC network. The voltage at the non-inverting terminal is

$$v_1 = \frac{\frac{1}{j2\pi fC}}{R+\frac{1}{j2\pi fC}} v_{in} = \frac{v_{in}}{1+j2\pi fCR}$$

The output voltage is

$$v_0 = \left(1+\frac{R_F}{R_1}\right) v_1 = (1+\frac{R_F}{R_1}) \frac{v_{in}}{1+j2\pi fCR}$$

Or, $v_o = \frac{A_f}{1+j(f/f_H)} v_{in}$

where A_F is the pass band gain of the filter and f_H is high cut-off frequency of the filter.

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_f}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} and\ \varphi = \tan^{-1}(f/f_H).$$

For, f < f_H , $|\frac{v_o}{v_{in}}| \cong A_F$; at f =f_H $|\frac{v_o}{v_{in}}| \cong \frac{A_F}{\sqrt{2}}$ = 0.707AF , at f > f_H $\left|\frac{v_o}{v_{in}}\right| < A_F$.

In designing low-pass active filter the value of C is generally taken less than 1 µF. First –order low-pass Butterworth filter provides a 20 dB/decade roll-off. To get 40 dB/decade roll-off a second –order low-pass Butterworth filter should be used.

Second-order low-pass Butterworth filter:

Schematic diagram of a second –order low-pas Butterworth filter is shown in circuit diagram 3.2.

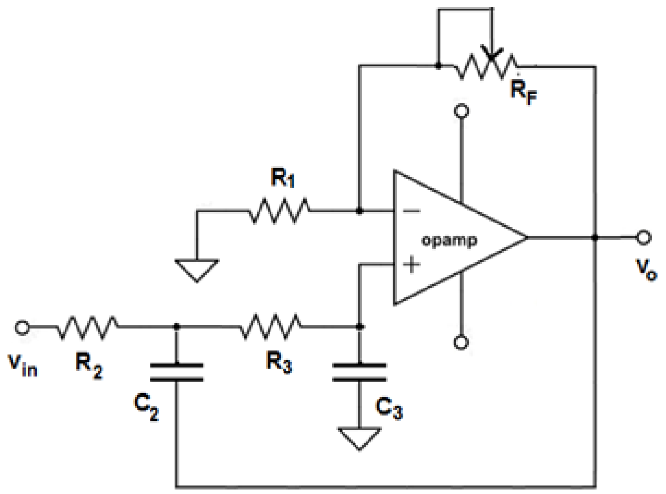


Fig.3.2 Circuit diagram of a second-order low-pass filter.

The cut-off frequency is

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

The gain of the filter is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_f}{\sqrt{1 + (f/f_H)^4}}$$

To design a second –order low-pas Butterworth filter we generally choose $R_2 = R_3 = R$, $C_2 = C_3 = C$ and $C \leq 1\mu F$. Therefore,

$$f_H = \frac{1}{2\pi RC}$$

To get a Butterworth response the gain of the filter should be equal to 1.586. Therefore

$$1 + \frac{R_F}{R_1} = 1.586$$

Or, $R_F = 0.586\ R_1$

Higher order low-pass filters, such as third order, fourth-order low-ass filters are formed simply using cascaded first and / or second order low-pass filters.

2. HIGH PASS FILTER

It is a network that allows the flow of signal with frequency above the cut-off frequency, f_L, and blocks the signals with frequency below the cut-off frequency. Here, few active high pass filters are realized by using Op-amp. Active high pass filters have the same principle of operation and frequency response as passive high pass filter, the only difference is that it uses an op-amp for amplification and gain control. The simplest form of an active high pass filter is a passive high pass filter connected at the input of an inverting /non-inverting amplifier.

Schematic diagrams of a first-order high-pass Butterworth filter are shown in circuit diagram 3.3 and 3.4, respectively. The filters can be achieved by interchanging the positions of the capacitors and resistors of a first-order and a second-order low pass Butterworth filter, respectively.

For the first order high pass Butterworth filter we have

$$v_o = \left(1 + \frac{R_F}{R_1}\right) v_1 = (1 + \frac{R_F}{R_1}) \frac{j2\pi fCR}{1+j2\pi fCR} v_{in}$$

Or, $v_o = A_F \frac{j(f/f_L)}{1+j(f/f_L)} v_{in}$

where A_F is the passband gain of the filter and f_L is low cutoff frequency of the filter. The gain of the first –order high-pass Butterworth filter is

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_f(f/f_L)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}}$$

Similarly, the gain of the second–order high-pass Butterworth filter is,

$$\left|\frac{v_o}{v_{in}}\right| = \frac{A_f(f/f_L)}{\sqrt{1 + \left(\frac{f}{f_L}\right)^4}}$$

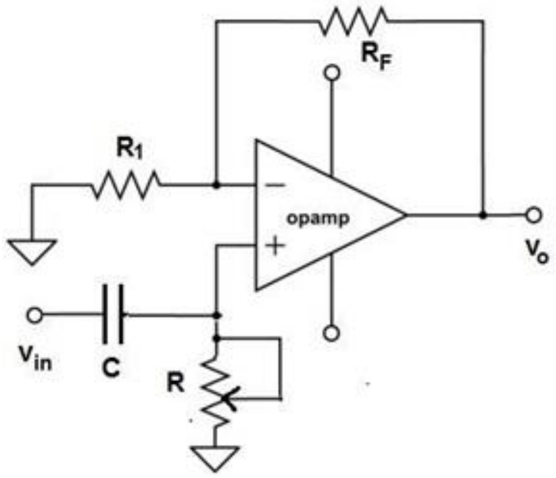


Fig.3.3 Circuit diagram of a first-order high pass Butterworth filter

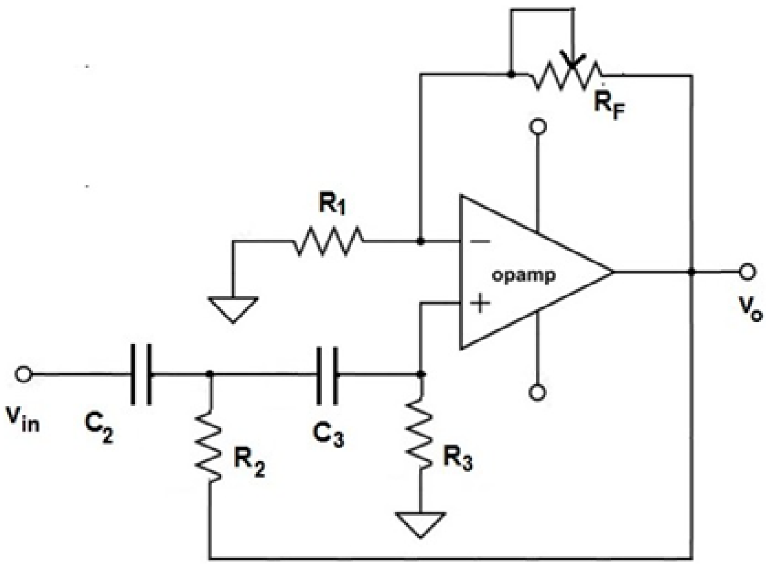


Fig.3.4 Circuit diagram of second-order high pass Butterworth filter

PROCEDURE

3. Derive / Check the component values [Typical values of resistors are in kΩ].
4. Setup the circuit on the breadboard / Multisim software and check the connections (for software simulation).
5. Apply suitable ac voltage levels and waveforms at the input terminal. [Typical values 1-2 V pp, Waveform: Sinusoidal.
6. For the frequency response of the low pass and high pass filters, vary the frequency of the input waveform and enter into the tabular column. Also plot the frequency curve.

OBSERVATION TABLE

TABLE - 1: FOR 1ST ORDER LOW PASS / 2ND ORDER LOW PASS / 1ST ORDER HIGH PASS / 2ND ORDER HIGH PASS FILTERS

Frequency (in Hz)	Input Voltage, Vi	Output Voltage, Vo	Gain (in dB)

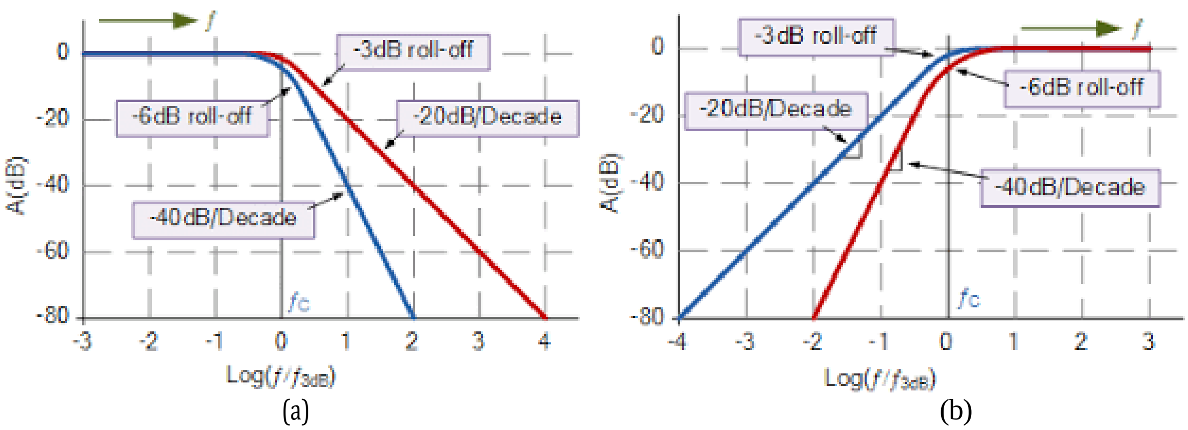


Fig. 3.5. Expected frequency Responses of (a) 1st and 2nd order low pass filter and (b) 1st and 2nd order high pass filter

OBJERVATIONS

Explain your result here.

CONCLUSION

1st and 2nd order active low pass and high pass filters have been design using OPAMP and there frequency responses have been studied.

TYPICAL QUESTIONS

1. Describe different pin configurations of IC741C.
2. What is the gain bandwidth product of OPAMP?
3. What are the general assumptions that we make during the design of an active filter using an OPAMP?
4. What are the characteristics of an ideal filter and a practical filter?
5. What is roll-off rate in filter design?

6. Design a 1^{st} order and 2^{nd} order HPF and LPF using op-amp circuit for cut-off frequency 5 kHz with Gain=2.
7. Design a 3rd order HPF and LPF using op-amp circuit for cut-off frequency 5 kHz with Gain=2.
8. How can you design higher order active low pass and high pass filters using the knowledge you gathered during the experiment?
9. How can you design a wide band active band pass filter using the knowledge you gathered during the experiment?
10. How can you design a wide band active band stop filter using the knowledge you gathered during the experiment?

OTHER RELATED OPAMP CIRCUIT DESIGN

1. Design of a third order and a fourth order active low pass filter using first order and / or second order active low pass filters.
2. Design of a third order and a fourth order active high pass filter using first order and / or second order active high pass filters.
3. Design of a first-order active wide-band band pass filter using a first order active low pass and a first order active high pass filters.
4. Design of an active narrow-band band pass filter using a single op amp.
5. Design of a first-order active wide-band band stop filter using a first order active low pass filter, a first order active high pass filter, and an adder circuit.
6. Design of an active narrow-band band stop filter using a single op amp.
7. Design of an active all pass filter using a single op amp.

EXPERIMENT – 04

GENERATION OF DIFFERENT WAVEFORMS USING OPAMP (Part I)

OBJECTIVE:

After completion of this experiment, student will be able to design OPAMP Comparator, Zero-Crossing detector, and Schmitt trigger Circuits.

APPARATUS AND COMPONENTS REQUIRED:

1. Dual power supply +/- 15 V
2. DC power source
3. Function Generator
4. Oscilloscope
5. Bread board (for hardware) / Multisim Software (Software)
6. IC 741C
7. Resistors
8. Capacitors
9. Probes and connecting wires

THEORY AND EXPLANATION

1. OPAMP Comparator

A comparator circuit compares a signal voltage applied at one input of an OPAMP with a known reference voltage at the other input. It is basically an open loop OPAMP with output $\pm V_{SAT}$. It is also called a voltage level detector because for the desired value of vref, the voltage level at the input can be detected. In general, comparators can be two types – non-inverting and inverting. The schematic diagram of a non-inverting comparator is shown in Fig. 4.1, where the input signal is fed at the non-inverting terminal of the OPAMP. In practical comparator circuit vref is obtained using a 10 kΩ potentiometer. When $v_{in} < V_{ref}$, the output voltage is at $-V_{SAT}$ because the voltage at inverting input is higher than at non-inverting input. When $v_{in} > V_{ref}$, the output voltage is at $+V_{SAT}$ because the voltage at inverting input is lower than at non-inverting input. The output waveform for a sinusoidal input signal is shown in Fig. 4.2. The schematic diagram of an inverting comparator and its output for a sinusoidal input are shown in Fig. 4.3 and Fig. 4.4. The diodes are used to protect the OPAMP from damage due to excessive input voltage. Because of these diodes, the difference in input voltage of the OPAMP is clamped either at +0.7 V or at -0.7 V. hence the diodes are called clamp diodes. The resistances are is used to limit the currents through the diodes. For OPAMPS with built in input protection the diodes can be removed.

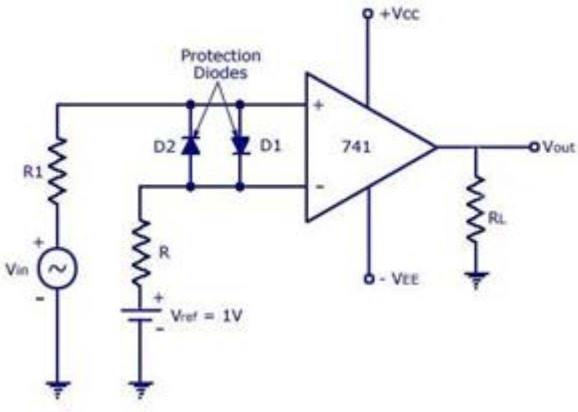


Fig. 4.1. Circuit diagram of a non-inverting comparator

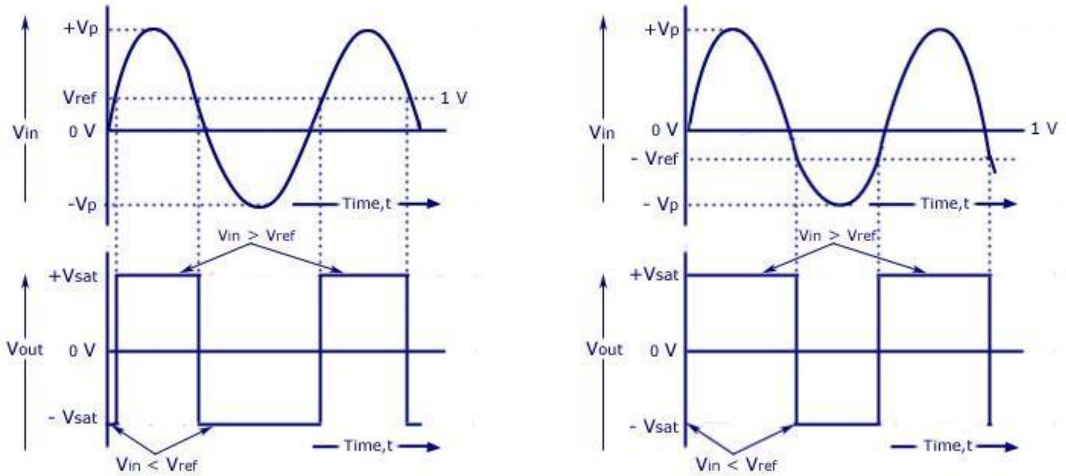


Fig. 4.2 Input and Output waveform of a non-inverting comparator

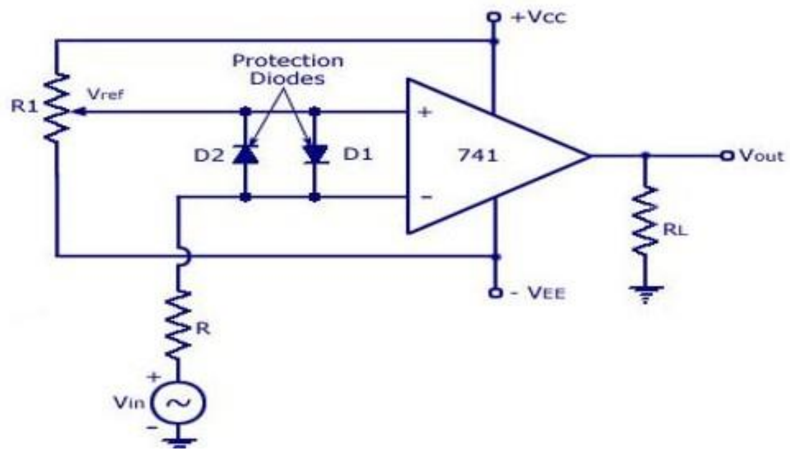


Fig. 4.3. Circuit diagram of an inverting comparator

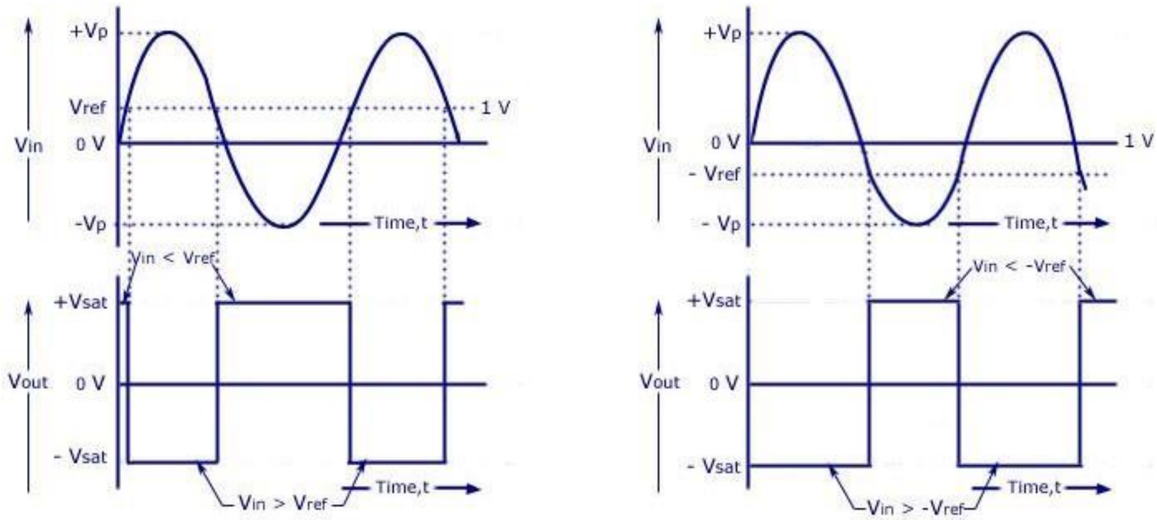


Fig. 4.4. Input and Output waveform of an inverting comparator

2. Zero-crossing detector

In zero-crossing detector (or sine wave to square wave converter) the V_{ref} is set to 0 V. When the input voltage passes to zero in positive direction the output is driven in to negative saturation. Conversely, when the input voltage passes to zero in negative direction the output is driven in to positive saturation. Because of the noise at the OPAMPs input terminals, the output voltage may fluctuate between two saturation voltages $+V_{SAT}$ and $-V_{SAT}$, detecting zero reference crossing for noise voltage as well as input voltage. Further if the input is a slowly varying waveform then input voltage will take more time to cross 0V.

Therefore output voltage may not switch quickly from one saturation voltage to another. These problems can be avoided with the use of regenerative or positive feedbac

3. **Schmitt Trigger**

Schematic diagram of Schmitt trigger circuit is shown in Fig.4.5. The resistance $R_{OM} = R_1 \| R_2$ is used to minimize the offset problem. The input voltage triggers (or changes the state of) the output every time it exceeds certain voltage levels, called upper threshold V_{ut} and lower threshold V_{lt}. The threshold voltages are obtained by using the voltage divider R_1-R_2, where the voltage across R_1 depends on the polarity of the output and is fed at the non-inverting input. Since the output voltage can be expressed as:

$$V_{ut} = \frac{R_1}{R_1 + R_2} V_{SAT}$$

And

$V_{lt} = \frac{R_1}{R_1+R_2} V_{SAT}$ respectively

In $v_{in} < v_{ut}$, the output remains constant at $+V_{sat}$. When v_{in} is just greater than v_{ut}, the output regeneratively switches to $-V_{SAT}$ and remains at this stage as long as $v_{in} > v_{lt}$. When $v_{in} < V_{lt}$, the output remains constant at $+V_{SA}$, till $V_{in} > V_{ut}$. These are shown in Fig.4.6. The figure shows that within v_{lt} and v_{ut} the output does not change state. The output changes its state only when $v_{in} < V_{lt}$ or $v_{in} > V_{ut}$. Therefore, if the threshold voltages are made larger than the input noise, the Schmitt trigger circuit can be eliminate false output transition. The positive feedback, because of its regenerative action, makes the output to switch faster between $+V_{SAT}$ or $-V_{SAT}$.

The comparator with positive feedback exhibit hysteresis, a dead-band condition, as shown. That is when the $v_{in} > V_{ut}$ its output switches from $+V_{SAT}$ or $-V_{SAT}$ and reverts back to its original state $+V_{SAT}$ when $v_{in} < V_{lt}$. The hysteresis voltage is the difference between v_{ut} and v_{lt} and is given by,

$$V_H = \frac{2R_1}{R_1 + R_2} V_{SAT}$$

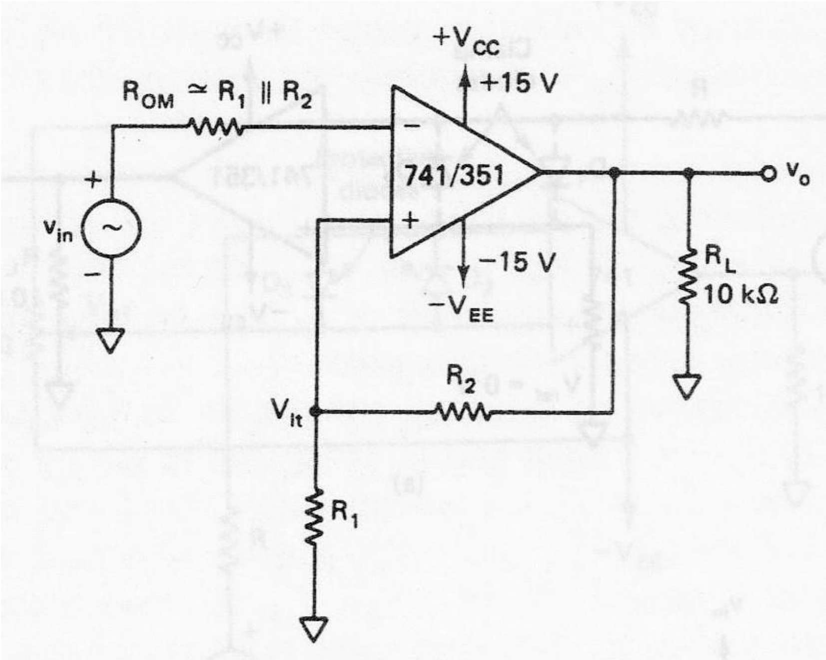
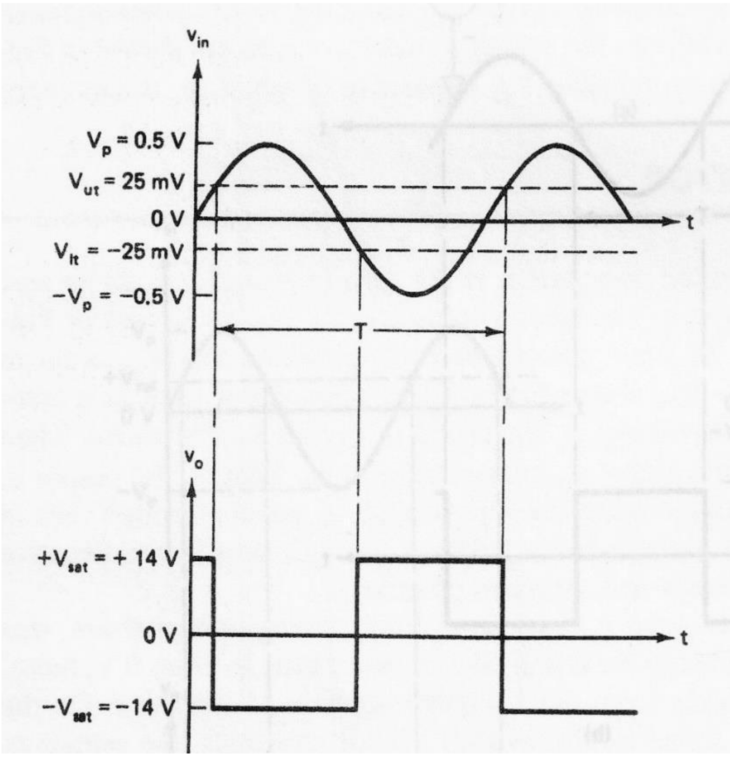
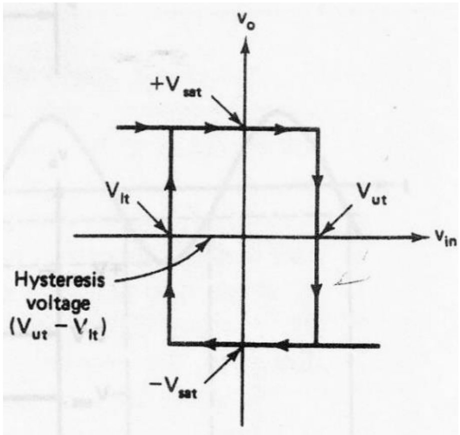


Fig. 4.5. Circuit diagram of a Schmitt Trigger.





(a) (b)

Fig. 4.6. (a) Input and Output waveform of a Schmitt Trigger and (b) Hysteresis in OPAMP Schmitt Trigger

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Setup the circuit on the breadboard / Multisim software and check the connections (for software simulation).
3. Connect the designated input to a sine wave signal generator with suitable peak to peak voltage at 1 – 2 kHz and remaining input with a suitable reference voltage (For comparators / zero-crossing detectors).
4. Plot the input waveform and output waveform on the same graph.
5. Plot hysteresis loop for the circuit (For Schmitt trigger circuit).

OBSERVATION TABLE:

TABLE-1: FOR COMPARATOR / ZERO-CROSSING DETECTOR /SCHMITT TRIGGER

Parameters	Input	Output
Voltage (Vp-p)		
Time period (ms)		

TABLE-2: FOR SCHMITT TRIGGER

Input Voltage	Output Voltage

CONCLUSION:

Non-inverting and inverting voltage comparators, zero crossing detector and Schmitt trigger circuits have been designed using op-amp and there output response have been studied.

TYPICAL QUESTIONS:

1. Why clamp diodes are used in comparator?
2. How to obtain high rate of accuracy in comparator?
3. How the op-amp comparator should be chosen to get higher speed of operation?
4. How to keep the output voltage swing of the op-amp comparator within specific limits?
5. What is the drawback in zero crossing detectors and state a method to overcome it.

6. Which circuit converts irregularly shaped waveform to regular shaped waveforms?
7. What happens if the threshold voltages are made higher than the noise voltages in Schmitt trigger?
8. In which configuration a dead band condition occurs in Schmitt trigger?
9. How to limit the output voltage swing only to positive direction?
10. What are the applications of Schmitt trigger?

EXPERIMENT – 05

GENERATION OF DIFFERENT WAVEFORMS USING OPAMP

(Part II)

OBJECTIVE:

After completion of this experiment, student will be able to design triangular wave and sine wave using OPAMP.

APPARATUS AND COMPONENTS REQUIRED:

1. Dual power supply +/- 15 V
2. DC power source
3. Oscilloscope
4. Bread board (for hardware) / Multisim Software (Software)
5. IC 741C
6. Resistors
7. Capacitors
8. Probes and connecting wires

THEORY AND EXPLANATION

I. Triangular Wave Generator

A triangular wave generator circuit is shown in Fig. 5.1. It consists of a comparator and an integrator. When the voltage at P goes slightly below or above 0 V, the output of the first OPAMP (A1) is at negative or positive saturation level, respectively. Let us assume the output of A1 is at positive saturation level $+V_{sat}$. This $+V_{sat}$ is an input of the integrator A2. The output of A2, therefore, will be a negative-going ramp. Thus one end of the voltage divide R_2–R_3 is at the positive saturation level of A1 and the other is the negative-going ramp of A2. When the negative-going ramp attains a certain value $-V_{Ramp}$, point P is slightly below 0 V; hence output of A1 will switch from positive saturation to negative saturation $-V_{sat}$. This means that output of A2 will now stop going negatively and will begin to go positively. The output of A2 will continue to increase until it reaches $+V_{Ramp}$. At this time point P is slightly above 0 V; therefore output of A1 switched back to the positive saturation level $+V_{sat}$.

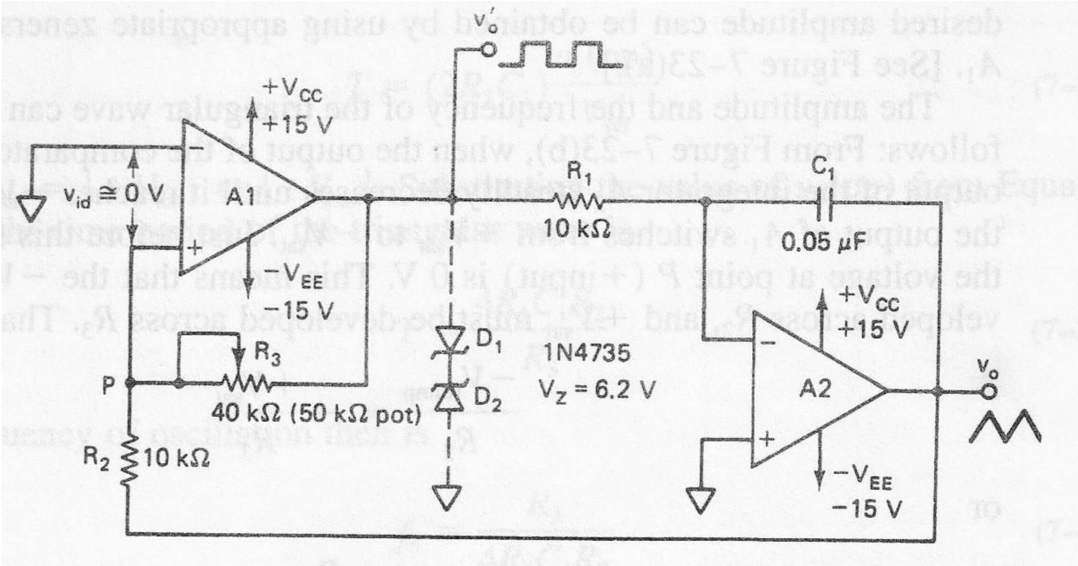


Fig. 5.1. Circuit diagram of a triangular wave generator

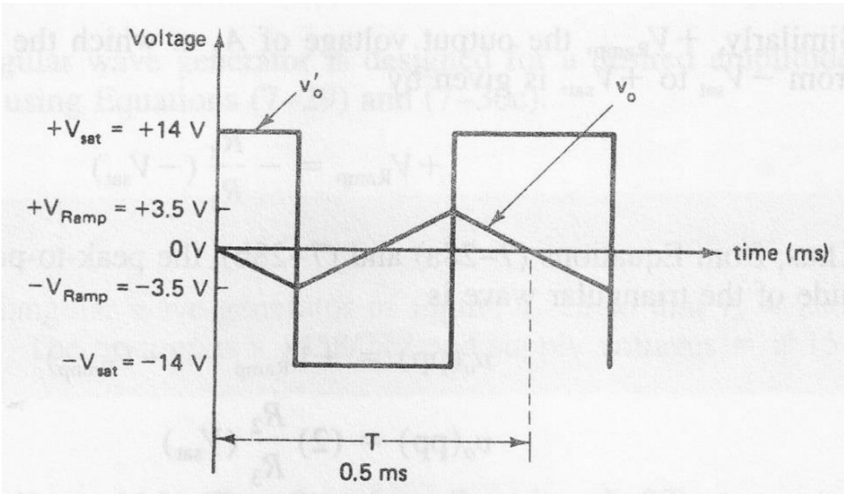


Fig. 5.2. Waveform a the output of the OPAMPs

The frequency of the square wave and triangular wave are same. The amplitude of the square wave is a function of dc supply voltages. However, a desired amplitude can be obtained by using appropriate Zeners at the output of A1, as shown. Just before the switching of output of A1 from $+V_{sat}$ to $-V_{sat}$, the voltage at P is 0 V. Therefore we can write,

$$-\frac{V_{Ramp}}{R_2} = -\frac{+V_{sat}}{R_3},$$

Or, $-V_{Ramp} = -\frac{R_2}{R_3}\left(+V_{sat}\right).$

Similarly,

$$+V_{Ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

Therefore peak-to-peak amplitude of the triangular wave is,

$$v_o(pp) = (+V_{Ramp}) - (-V_{Ramp}) = \left(-\frac{R_2}{R_3}(-V_{sat})\right) - \left(-\frac{R_2}{R_3}(+V_{sat})\right) = \frac{2R_2}{R_3}(+V_{sat})$$

The time taken by the output to swing from $-V_{Ramp}$ to $+V_{Ramp}$ is equal to the half of the time period T/2. Therefore,

$$v_o(pp) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})dt = \frac{V_{sat}}{R_1C_1}\frac{T}{2}$$

Or, $T = 2R_1C_1\frac{v_o(pp)}{V_{sat}} = \frac{2R_1C_1}{V_{sat}}\frac{2R_2V_{sat}}{R_3} = \frac{4R_1C_1R_2}{R_3}$.

The frequency of oscillation is $f_o = \frac{R_3}{4R_1C_1R_2}$.

II. RC- Phase Shift Oscillator

Schematic diagram of an OPAMP phase shift oscillator is shown in Fig. 5.3. In the circuit the OPAMP has been used in the inverting mode; therefore, any signal that appears at the inverting terminal is shifted by 180^o at the output. At the resonance frequency f_o = 0.065/RC, the cascaded RC network provides another 180^o phase shift; thus the total phase shift around the loop becomes 360^o or 0^o. At this frequency the gain of the amplifier must be at least 29, (i.e., R_F= 29R_1). To avoid loading effect we must set $R_1 \geq 10R$. A desired output can be obtained by using back-to-back Zener diode, as shown.

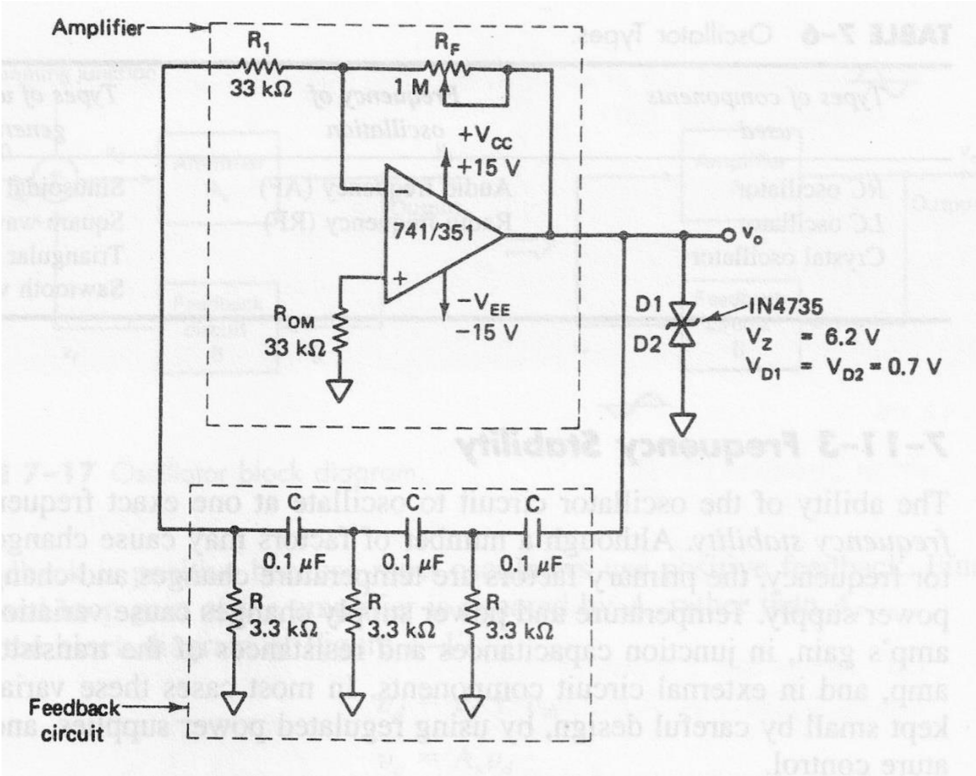


Fig. 5.3 Circuit diagram of a RC phase shift oscillator

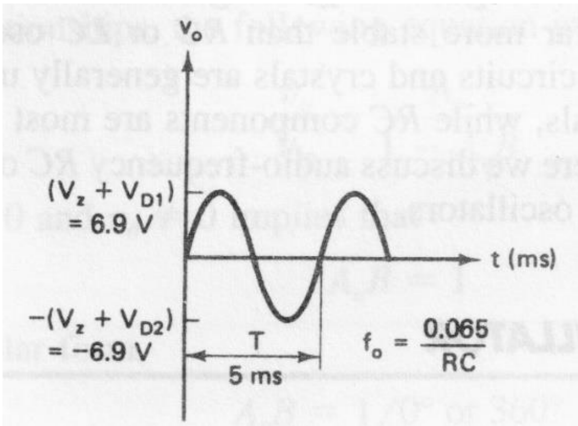


Fig. 5.4. Output waveform of the RC phase shift oscillator

PROCEDURE:

1. Connect the circuit as shown in the Fig. 5.1 / Fig. 5.3 on the breadboard / Multisim software (for software simulation) and check the connections. You can initially neglect the diodes.
2. Connect the CRO at the outputs of the OPAMPs and ensure the correct waveforms at the respective outputs.

3. Plot the output waveforms of the OPAMPs.
4. Note the frequency / time periods the waveforms and compare them with the theoretical values.

OBSERVATION TABLE:

TABLE-1: FOR SQUARE/TRIANGULAR WAVE GENERATOR.

Parameters	Square Wave Output	Triangular Wave Output
Voltage Amplitude (Vp-p)		
Time period (ms)		

TABLE-2: FOR RC PHASE SHIFT OSCILLATOR.

Parameters	Sinusoidal Output
Voltage Amplitude (Vp-p)	
Time period (ms)	
Frequency (f_O)	
Comparison with theoretical frequency (f_O=0.065/RC).	

CONCLUSION:

Different waveforms have been generated through designed waveform generator circuits. Triangular wave is generated by the triangular wave generator, whereas sinusoidal wave is generated through designed RC phase shift oscillator circuit using Op-Amp.

TYPICAL QUESTIONS:

1. What will happen if a fixed reference voltage, instead of ground, is connected at non-inverting terminal of integrator in Fig. 5.1?
2. How can the rise and fall time of triangular waveform be made unequal?
3. How the increase in the frequency of triangular wave will affect the magnitude of output waveform?
4. What is slew rate of a waveform generator circuit?
5. Why 3 RC network stages are used in phase shift oscillator?
6. What is Bark-hausen criterion for oscillation?
7. What is an oscillator?
8. How can you control the frequency of the triangular wave in a triangular wave generator?
9. What is the function of the diodes in the triangular and RC-phase shift oscillator?
10. How do you calculate the values of R and C in a RC-phase shift oscillator?

OTHER RELATED OPAMP CIRCUIT DESIGN:

1. Design a triangular wave generator using a Schmitt-trigger and an integrator circuit.
2. Design a saw-tooth wave generator.
3. Design a Wien Bridge oscillator.
4. Design a quadrature Oscillator.

EXPERIMENT – 06

DESIGN A COMMON EMITTER AMPLIFIER WITH PROPER Q-POINT SETTING AND STUDY THE FREQUENCY RESPONSE OF THE AMPLIFIER.

OBJECTIVE:

After completing this experiment, the student will be able to design and set up a common emitter amplifier with proper Q-point setting and study its frequency response.

APPARATUS AND COMPONENTS REQUIRED:

1. Regulated DC power supply.
2. Function generator
3. Oscilloscope
4. Breadboard (For Hardware) / Multisim Software (Software)
5. Resistor
6. Capacitor
7. Bipolar Junction Transistor

THEORY AND EXPLANATION:

An amplifier is a device that amplifies the weak electric signals. One of the most common application of BJT is as an amplifier. For the BJT to act as an amplifier, it must be operated in the middle of the active region. A typical circuit diagram for a small signal common emitter (CE) amplifier is shown in Fig. 6.1. In this arrangement, potential divider bias has been used, which has the highest stability factor against variation of *beta, β*. The component values are such that it will drive the transistor into the active region. The emitter resistance further improves the stability and provides negative feedback to the base-emitter loop that reduces the overall gain of the transistor. A small signal to be amplified is connected to the base-emitter loop through coupling capacitor. The capacitors in the circuit block the dc signal therefore the operating point remains unchanged. The capacitor across the emitter resistance bypasses the ac signal and improves the amplifier's gain. Apart from the external capacitances, the BJT also have internal capacitances at the junctions. The presence of all these capacitance in the circuit makes the overall gain frequency-dependent.

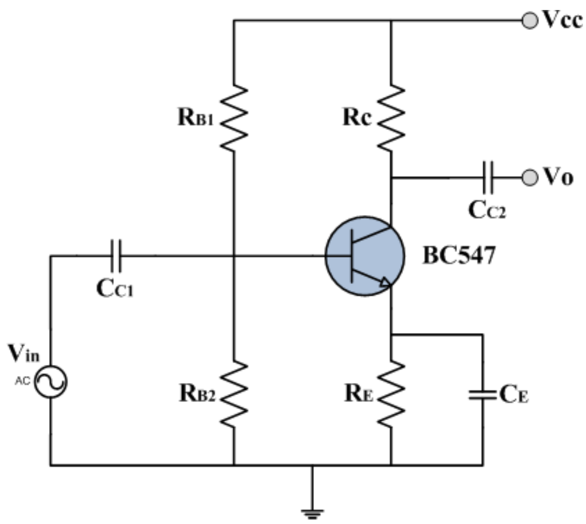


Fig 6.1. Circuit diagram of common emitter amplifier

AMPLIFIER OPERATION

Once the Q-point is fixed through DC bias, a sinusoidal signal is applied at the input through the coupling capacitor $CC1$. During the positive half cycle of the input signal V_{BE} increases leading to an increased I . Therefore I_c increases by β times which reduces the output voltage, V_0 as $V_0 = V_{CC} - I_C R_C$. Similarly, during the negative half cycle, I_c decreases which increases the output voltage. Thus the CE amplifier produces an amplified output with a phase reversal.

FREQUENCY RESPONSE CURVE

An amplifier's performance is characterized by its frequency response curve that shows gain (dB) plotted against frequency. Fig 6.2 shows the typical frequency response characteristics of a CE amplifier. The frequency response of an amplifier can be divided into three frequency ranges. The curve is flat for the mid-range of frequencies. In the low-frequency range between 0 Hz and lower cutoff frequency, the external coupling and bypass capacitors decide the gain. However, at higher frequencies, the internal capacitances of the transistor play a significant role. The difference between lower and higher cutoff frequencies is called the bandwidth.

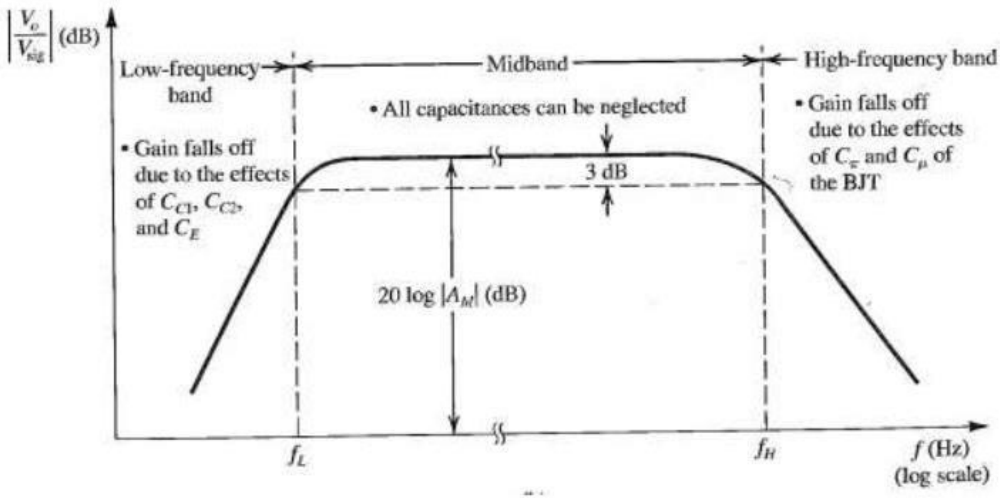


Fig. 6.2. Frequency response: Gain versus frequency plot

CIRCUIT DESIGN:

Calculating the resistances:

The quiescent operating point or Q-point must be set at the centre position of load line for any small-signal amplifier to generate an amplified output with minimum distortion. Fig. 6.3 shows the voltage divider bias configuration. For the Q-point to be in the middle of the active region, V_{CE} should be 50% of V_{CC}.

To control the negative feedback, R_E should be sufficiently low. Ideally, $R_C = 4R_E$. Hence, $V_{CE} = 0.5\ V_{CC}$, $V_E = 0.1\ V_{CC}$, and $V_C = 0.4\ V_{CC}$.

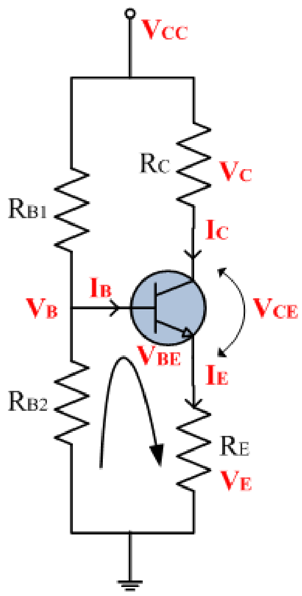


Fig. 6.3. Voltage divider bias configuration

In the input section of voltage divider bias configuration, the equivalent resistance between base and ground is defined by $R_i = (\beta + 1)R_E$. The sensitivity to changes in β is relatively small if the value of R_{B2} is at least 10 times smaller than R_i, i.e, $R_{B2} < 0.1\ (\beta+1)\ R_E$.

Applying KVL to the base –emitter loop of the transistor as shown in Fig.6.3,

$$V_B = V_{BE} + V_E$$

$$or\ \frac{V_{CC}R_{B2}}{R_{B1}+R_{B2}} = V_{BE} + V_E$$

$$so\ that\ R_{B1} = \frac{V_{CC}R_{B2}}{V_{BE}+V_E} - R_{B2}$$

Calculating coupling capacitors C_{C1} and C_{C2}:

Coupling capacitors C_{C1} and C_{C2} are used to separate the AC signals from the DC biasing voltage, so that the Q-point of the circuit remains undisturbed when input AC signal is applied.

The reactance X_{C1} of coupling capacitor C_{C1} should be less than the input resistance, R_{in} of the transistor.

$$X_{C1} \le \frac{R_{in}}{10}$$

Here $R_{in} = R_{B1} \parallel R_{B2} \parallel \beta r_e$

Where $r_e (= \frac{26mV}{I_E})$ is the ac emitter resistance. The equivalent input (R_{in}) and output (R_{out}) resistance of the transistor are shown in Fig.6.4

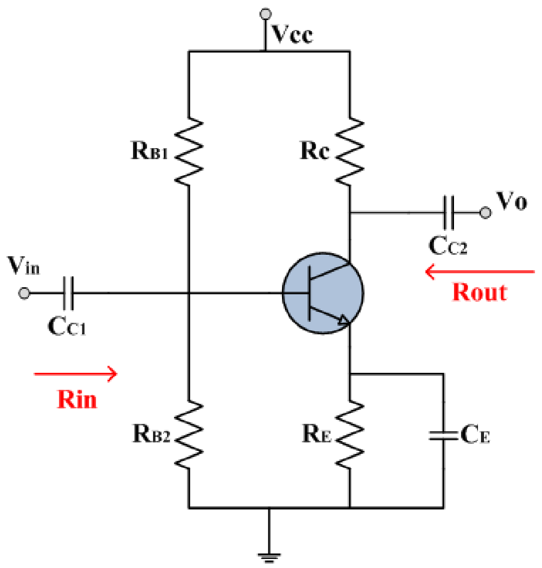


Fig. 6.4. Circuit of CE amplifier showing input and output resistance.

For a lower cut-off frequency of f_L Hz:

$$C_{C1} = \frac{1}{2\pi f_L X_{C1}}$$

The reactance X_{C2} of coupling capacitor C_{C2} should be less than the output resistance, R_{out} of the transistor.

$$X_{C2} \leq \frac{R_{out}}{10}$$

Here, $R_{out} = R_C$

$$So, C_{C2} = \frac{1}{2\pi f_L X_{C2}}$$

Calculating bypass capacitors C_E:

To bypass the lowest frequency, X_{CE} should be much less than or equal to the resistance R_E.

$$X_{CE} \leq \frac{R_E}{10}$$

So, $C_E = \frac{1}{2\pi f_L X_{CE}}$

PROCEDURE:

1. Assume VCC, β, and RE to calculate the value of rest of the components.
2. Set up the circuit on the breadboard / Multisim software and check the connections.
3. Apply suitable AC voltage levels at the input terminal. [Typical values 10-20 mV pp, Waveform: Sinusoidal]
4. Observe input and output on two channels of the oscilloscope simultaneously.
5. Note down the value of output voltage by varying the frequency from 10Hz to 10GHz.
6. Calculate the voltage gain (in dB) for each frequency.
7. Plot the frequency response curve, i.e., gain in dB versus frequency on a semilog graph-sheet.
8. Estimate the mid-frequency gain, the lower and higher cutoff frequencies, and hence the bandwidth.

OBSERVATION TABLE:

To obtain the frequency response:

Fix the input amplitude and vary the frequency from 10Hz-10GHz and note down the output amplitude.

Sl. No.	Frequency (Hz)	Output voltage (Volt)	Gain (V_0/V_i)	Gain (dB)

OBSERVATIONS:

Explain your result here.

CONCLUSION

A CE amplifier with proper Q-point setting has been designed, and its frequency response has been studied. The upper and the lower 3dB cutoff frequencies are identified and marked on the response curve.

TYPICAL QUESTIONS:

1. What are the advantages of common emitter amplifier circuit over other BJT amplifier circuits?
2. What are the applications of a common emitter amplifier?
3. Find the input impedance of a CE amplifier circuit.
4. Find the output impedance of a CE amplifier circuit.
5. Explain the significance of emitter resistance in the design of CE amplifier.
6. Explain the effect of a bypass capacitor on the passband gain of CE amplifier.
7. Explain the phase relationship between the input and output signals of CE amplifier.

OTHER RELATED BJT CIRCUIT DESIGN:

1. Common base amplifier
2. Common collector amplifier
3. CE fixed base bias circuit
4. CE emitter-bias circuit
5. Collector to base bias circuit

EXPERIMENT – 07

PERFORMANCE ANALYSIS (FREQUENCY RESPONSE) OF CASCADED AMPLIFIERS.

OBJECTIVE:

After completing this experiment, the student will be able to design and set up a cascaded amplifier and study its frequency response.

APPARATUS AND COMPONENTS REQUIRED:

1. Regulated DC power supply.
2. Function generator
3. Oscilloscope
4. Breadboard (For Hardware) / Multisim Software (Software)
5. Resistor
6. Capacitor
7. Bipolar Junction Transistor

THEORY AND EXPLANATION:

An amplifier is a device that amplifies the weak electric signals. One of the most common application of BJT is as an amplifier. For the BJT to act as an amplifier, it must be operated in the middle of the active region.

Multistage amplifier

A single stage of amplification is often not enough for a particular application. For that, we have to use multiple stages of amplification for achieving the required voltage gain or power. This kind of amplifier is termed as a multistage amplifier analysis. In this amplifier, the first stage output is fed to the next stage input. Such type of connection is commonly known as cascading. RC coupled amplifier usually employed for voltage amplification. It consists of a coupling capacitor which is used to connect the output of the first stage to the base (i.e input) of the next stage. The resistors R_1, R_2, R_E forms the biasing and stabilizing network. The emitter bypass capacitor offers low resistance path to the signal. Without it, the voltage gain of the each stage would be lost. The coupling capacitor blocks DC and allows AC therefore this prevents the DC interference between the various stages and the shifting of operating point. A typical circuit diagram for a multistage (cascaded) common emitter (CE) amplifier is shown in Fig. 6.1.

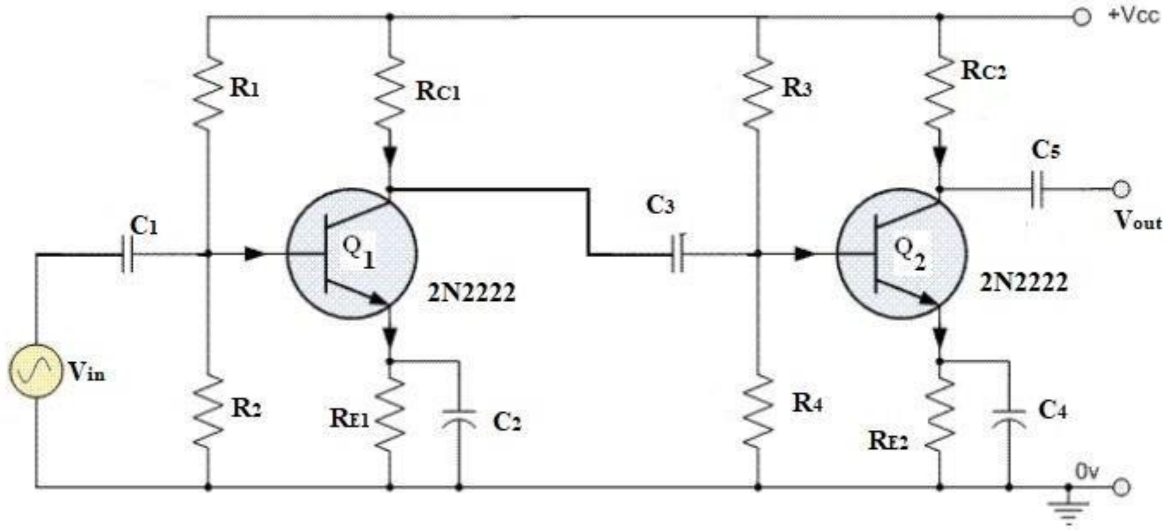


Fig 7.1. Circuit diagram of cascaded common emitter amplifier

Operation: When AC signal is applied to the base of the first transistor, it appears in the amplified form across its collector load R_c. the amplified signal developed across R_c is given to the next stage through coupling capacitor. The second stage does further amplification of the signal, in this way the cascaded stages amplify the signal and the overall gain is considerably increased and the bandwidth decreases. Capacitors C_1 and C_3 couple the input signal to transistors Q_1 and Q_2, respectively. C5 is used for coupling the signal from Q_2 to its load. R_1, R_2, RE1 and R_3, R_4, RE2 are used for biasing and stabilization of stage 1 and 2 of the amplifier. C2 and C4 provide low reactance paths to the signal through the emitter.

<u>Overall gain:</u>

The total gain of a 2-stage amplifier is equal to the product of individual gain of each stage. Once the second stage is added, its input impedance acts as an additional load on the first stage thereby reducing the gain as compared to its no load gain. Thus the overall gain characteristics is affected due to this loading effect.

The loading of the second stage, i.e. input impedance of second stage, $Z_{i2} = R_3 \parallel R_4 \parallel \beta r_{e2}$ Thus loaded gain of the first stage, $A_{V1} = -(R_C \parallel Z_{i2})/ r_{e2}$

And, the unloaded gain of second stage, $A_{V2} = - R_{C2} / r_{e2}$

The overall gain of the 2 stage amplifier is, $A_{V1} = A_{V1} \times A_{V2}$

FREQUENCY RESPONSE CURVE

An amplifier's performance is characterized by its frequency response curve that shows gain (dB) plotted against frequency. Fig 6.2 shows the typical frequency response characteristics of a CE amplifier. The frequency response of an amplifier can be divided into three frequency ranges. The curve is flat for the mid-range of frequencies. In the low-frequency range between 0 Hz and lower cut-off frequency, the external coupling and bypass capacitors decide the gain. However, at higher frequencies, the internal capacitances of the transistor play a significant role. The difference between lower and higher cut-off frequencies is called the bandwidth.

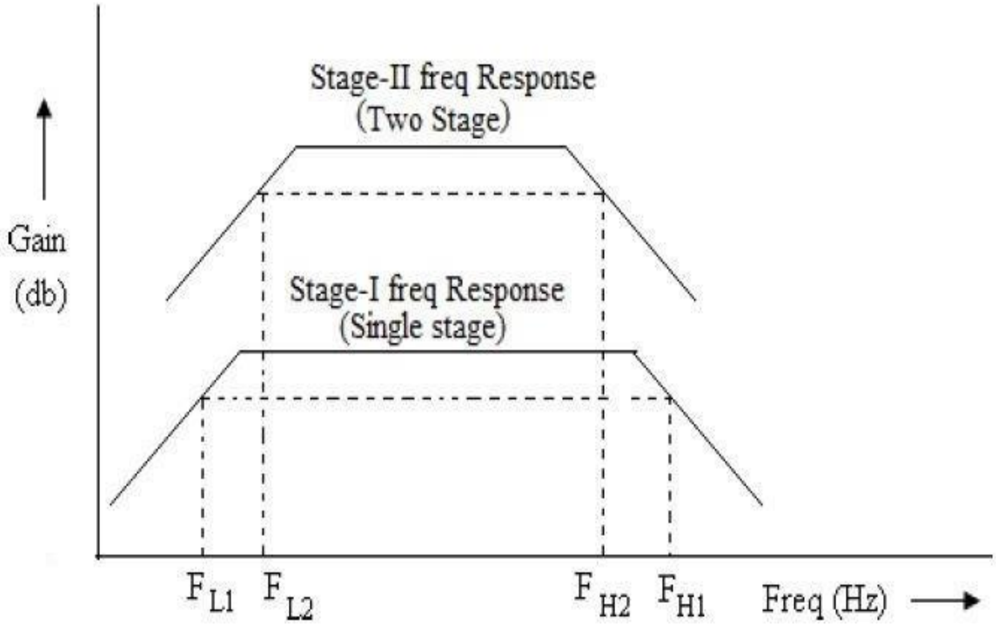


Fig. 7.2. Frequency response: Gain versus frequency plot

<u>CIRCUIT DESIGN</u>:

For individual stage:

Calculating the resistances:

The quiescent operating point or Q-point must be set at the center position of load line for any small-signal amplifier to generate an amplified output with minimum distortion. Fig. 6.3 shows the voltage divider bias configuration. For the Q-point to be in the middle of the active region, VCE should be 50% of VCC.

To control the negative feedback, RE should be sufficiently low. Ideally, $R_C = 4R_E$. Hence, $V_{CE} = 0.5\ V_{CC}$, $V_E = 0.1\ V_{CC}$, and $V_C = 0.4\ V_{CC}$.

For 2N222 transistor, Put β=100.

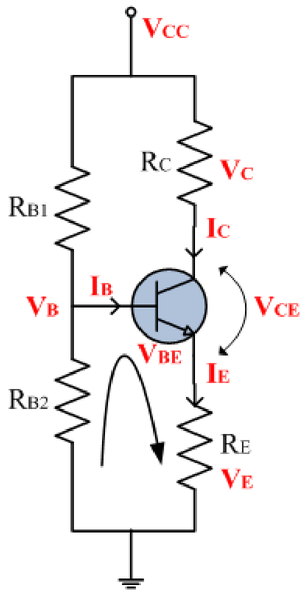


Fig. 7.3. Voltage divider bias configuration

In the input section of voltage divider bias configuration, the equivalent resistance between base and ground is defined by $R_i = (\beta+1)R_E$. The sensitivity to changes in β is relatively small if the value of R_{B2} is at least 10 times smaller than R_i, i.e., $R_{B2} < 0.1(\beta+1)R_E$.

Applying KVL to the base-emitter loop of the transistor,

$$V_B = V_{BE} + V_E$$

$$or \; \frac{V_{CC}R_{B2}}{R_{B1} + R_{B2}} = V_{BE} + V_E$$

$$so\ that\ R_{B1} = \frac{V_{CC}R_{B2}}{V_{BE} + V_E} - R_{B2}$$

Calculating coupling capacitors C_{C1} and C_{C2}:

Coupling capacitors C_{C1} and C_{C2} are used to separate the AC signals from the DC biasing voltage, so that the Q-point of the circuit remains undisturbed when input AC signal is applied.

The reactance X_{C1} of coupling capacitor C_{C1} should be less than the input resistance, R_{in} of the transistor.

$$X_{C1} \leq \frac{R_{in}}{10}$$

Here $R_{in} = R_{B1} \parallel R_{B2} \parallel \beta r_e$

Where $r_e (= \frac{26mV}{I_E})$ is the ac emitter resistance. The equivalent input (R_{in}) and output (R_{out}) resistance of the transistor are shown in Fig.7.4

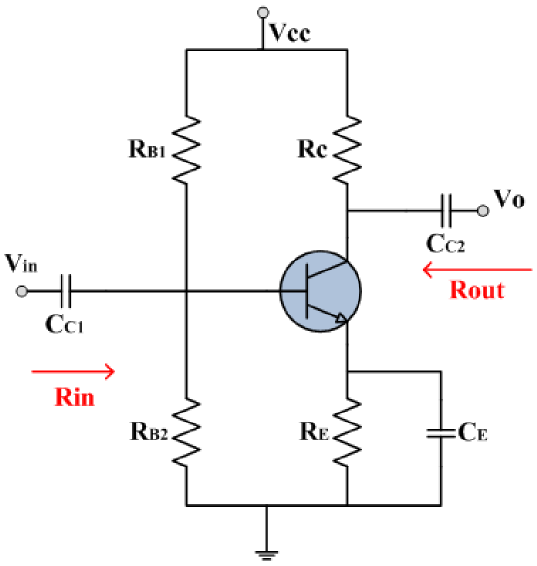


Fig.7.4 Circuit of CE amplifier showing input and output resistance.

For a lower cut-off frequency of f_L Hz:

$$C_{C1} = \frac{1}{2\pi f_L X_{C1}}$$

The reactance X_{C2} of coupling capacitor C_{C2} should be less than the output resistance, R_{out} of the transistor.

$$X_{C2} \leq \frac{R_{out}}{10}$$

Here, $R_{out} = R_C$

$$So, C_{C2} = \frac{1}{2\pi f_L X_{C2}}$$

Calculating bypass capacitors C_E:

To bypass the lowest frequency, X_{CE} should be much less than or equal to the resistance R_E.

$$X_{CE} \leq \frac{R_E}{10}$$

So, $C_E = \frac{1}{2\pi f_L X_{CE}}$

PROCEDURE:

1. Assume VCC, β (=100, as transistor 2N2222 range between 50-200), and RE to calculate the value of rest of the components.
2. Set up the circuit on the breadboard / Multisim software and check the connections.
3. Apply suitable AC voltage levels at the input terminal. [Typical values 10-20 mV pp, Waveform: Sinusoidal]
4. Observe input and output on two channels of the oscilloscope simultaneously.
5. Note down the value of output voltage by varying the frequency from 10Hz to 10GHz.
6. Calculate the voltage gain (in dB) for each frequency.
7. Plot the frequency response curve, i.e., gain in dB versus frequency on a semilog graph-sheet.
8. Estimate the mid-frequency gain, the lower and higher cutoff frequencies, and hence the bandwidth.

OBSERVATION TABLE:

To obtain the frequency response:

Fix the input amplitude and vary the frequency from 10Hz-10GHz and note down the output amplitude.

Sl. No.	Frequency (Hz)	Output voltage (Volt)	Gain (V0/Vi)	Gain (dB)

OBSERVATIONS:

Explain your result here.

CONCLUSION

A multistage CE amplifier with proper Q-point setting has been designed, and its frequency response has been studied. The upper and the lower 3dB cutoff frequencies are identified and marked on the response curve.

EXPERIMENT – 08

DRAIN AND TRANSFER CHARACTERISTIC OF FIELD EFFECT TRANSISTOR (FET)

OBJECTIVE:

To conduct experiment to study the transfer and drain characteristics of a JFET and determine its parameters.

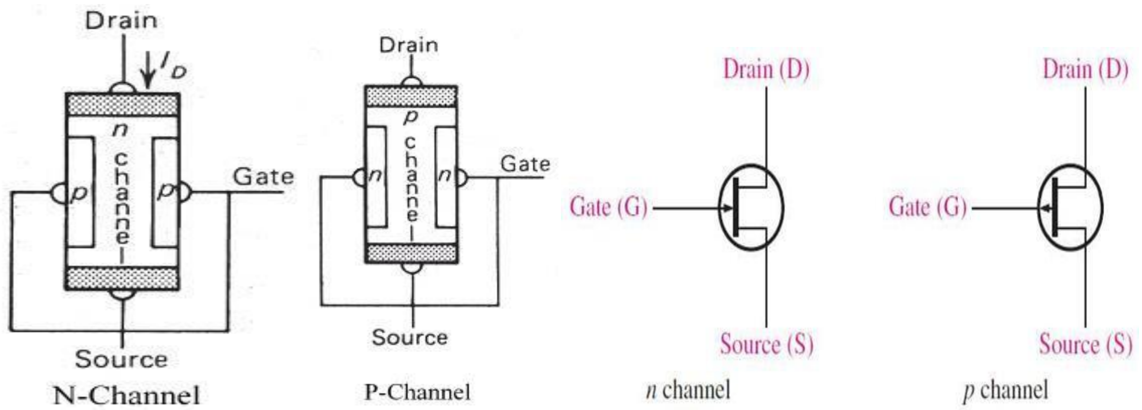
APPARATUS AND COMPONENTS REQUIRED:

1. JFET(NPN) Q1A2N5454
2. Resistor (10K)
3. Variable power supply
4. Breadboard (For Hardware) / Multisim Software(Software)

THEORY AND EXPLANATION:

JFET

The JFET (Junction Field-Effect Transistor) is a type of FET that operates with a reverse-biased p-n junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel. In n- channel JFET the drain is at the upper end, and the source is at the lower end. Two p-type regions are diffused in the n-type material to form a channel, and both p-type regions are connected to the gate lead. For simplicity, the gate lead is shown connected to only one of the p regions. The inverse of n-channel JFET is p-channel JFET.



Transfer characteristics: The range of VGS values from zero to VGS (off) controls the amount of drain current. For an n-channel JFET, VGS (off) is negative, and for a p-channel JFET, VGS (off) is positive. Because VGS does control ID, the relationship between these two quantities is very important. This curve is also known as a transconductance curve

Drain saturation current IDSS: Maximum current flowing through JFET when gate to source voltage is zero.

Pinch-off voltage VP: Gate to source voltage at which, drain current becomes zero.

Transconductance gm: The forward transconductance (transfer conductance), is the change in drain current ID for a given change in gate- to-source voltage IGS with the drain-to-source voltage VDS constant.

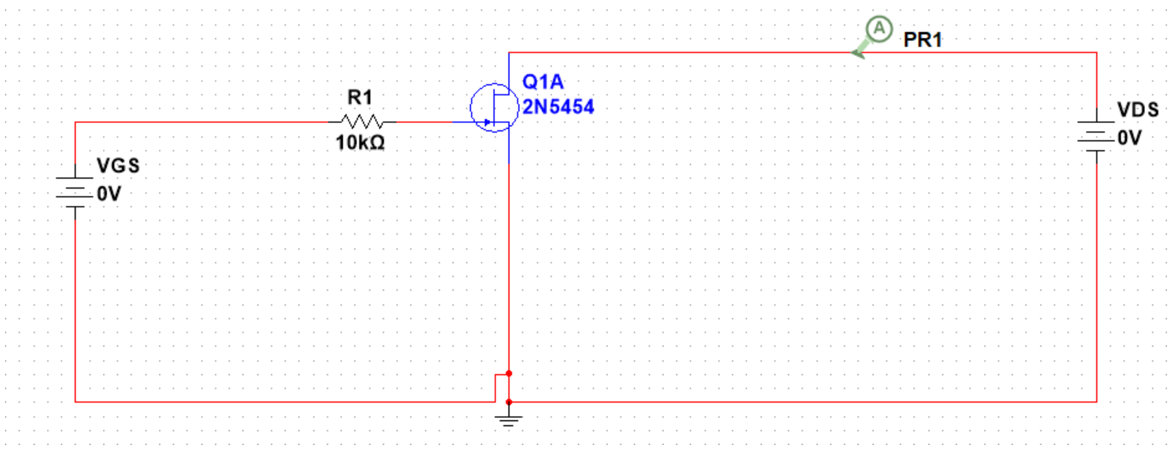
$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\bigg|_{V_{DS}\ constant}$$

Drain characteristics: The curve between drain current ID and drain-source voltage VDS of a JFET at constant gate-source voltage VGS is known as drain characteristics of JFET.

Drain dynamic resistance rd: The drain dynamic resistance is defined as the ratio of change in drain to source voltage VDS to the change in drain current ID, when gate to source volt age remain constant.

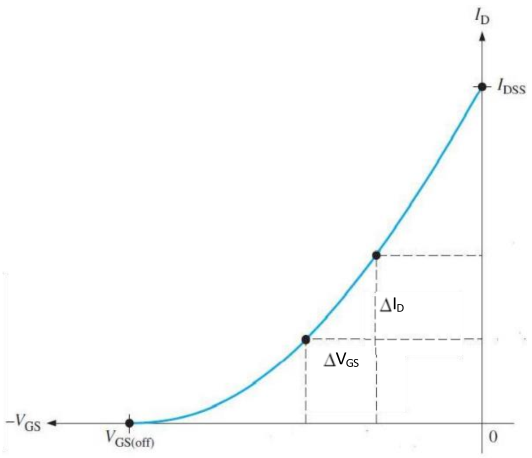
$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}\ constant}$$

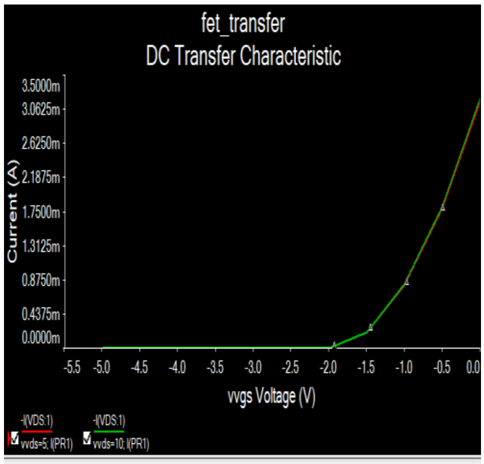
CIRCUIT DIAGRAM:



Transfer Characteristics Observations:

Transfer Characteristics			
V_{DS}= 15V		V_{DS}= 30V	
V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)





CALCULATION

Drain saturation current I_{DSS} =

Pinch-off voltage V_P=

Transconductance $g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\ constant}$

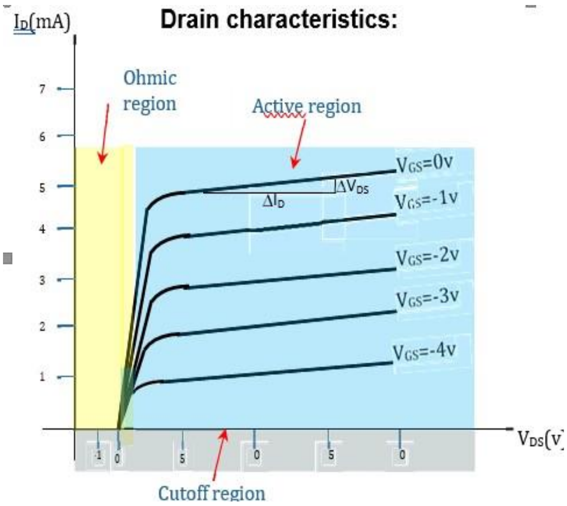
PROCEDURE:

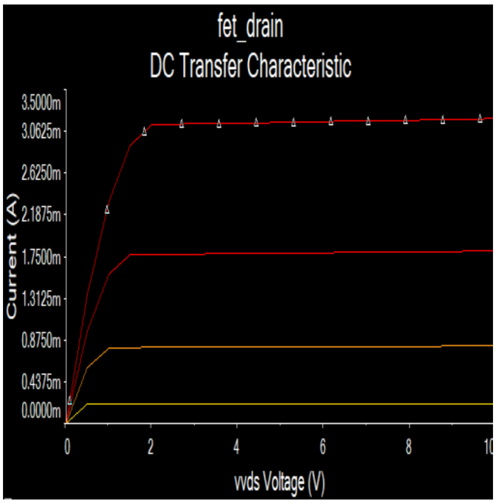
1. Connect the circuit as per given diagram properly.
2. Set the voltage VDS constant at 30 V.
3. Vary VGS in the step of -5 V up to 0V in step 0.5 and note down value of drain current ID. Tabulate all the readings.

4. Repeat the same procedure for VDS= 15V
5. Plot transfer characteristics VGS vs ID for constant VDS.
6. Calculate IDSS, VGS (off), gm from the graphs and verify.

Drain Characteristics Observations:

Drain Characteristics					
V_{GS}= 0V		V_{GS}= -1V		V_{GS}= -2V	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D(mA)	V_{DS} (V)	I_D (mA)





Calculations:

Drain dynamic resistance $r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}\ constant}$

Procedure:

1. Connect the circuit as per given diagram properly.
2. Keep VGS = 0V and vary VDS

3. Vary V_{DS} in step of -1V from 0 volts up to -3 volts and measure the drain current I_D. Tabulate all the readings.
4. Repeat the above procedure for V_{GS} as -1V, -2V, -3Vetc.
5. Calculate r_d from the graphs and verify.

CONCLUSION:

Drain and transfer characteristics have been obtained for N channel JFET also we have evaluated transconductance and drain resistance for the N channel JFET.

TYPICAL QUESTIONS:

1. What are the advantages of FET?
2. Different between FET and BJT?
3. Explain different regions of V-I characteristics of FET?
4. What are the applications of FET?
5. What are the types of FET?
6. Draw the symbol of FET.
7. What are the disadvantages of FET?
8. What are the parameters of FET?

EXPERIMENT N0: 09

REALIZATION OF CURRENT MIRROR CIRCUIT

OBJECTIVE:

To conduct an experiment for the realization of current mirror circuit.

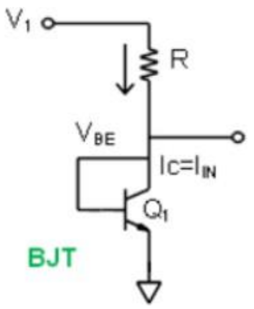
APPARATUS AND COMPONENTS REQUIRED:

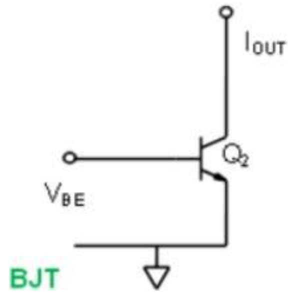
1. Bread board
2. Regulated power supply
3. DSO
4. Transistor (Q_1 and Q_2, any transistor with higher gain)
5. Resistors (R_2 = 4.7 K to 10 K ohm and R_L = 0.100 K to 10 K ohm)
6. Connecting wires
7. Multimeter
8. Multisim software

THEORY:

A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. The simple two transistor implementation of the current mirror is based on the fundamental relationship that two equal size transistors at the same temperature with the same V_{GS} for a MOS or V_{BE} for a BJT have the same drain or collector current.

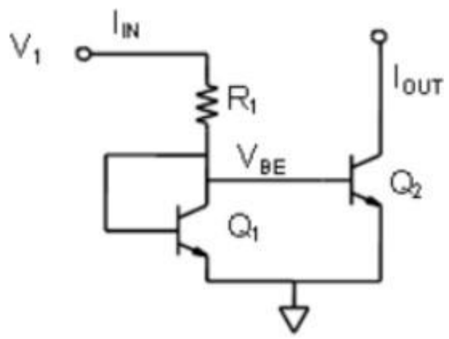
We would like a simple configuration where the active element, a single transistor, serves as the desired current-to-voltage converter. However, the transistor is a unidirectional device, where for the BJT the base emitter voltage controls the collector current.





A bipolar transistor can be driven by a voltage or by a current. The collector provides the output terminal of our simple current mirror: The output V to I converter stage of the simple current mirror is just a transistor acting as a non-linear (exponential for BJT) voltage-to-current converter.

The final step is to connect the output of the input stage (the base emitter junction of Q_1) to the input of the output stage (the base emitter junction of Q_2) to build the basic BJT current mirror circuit.

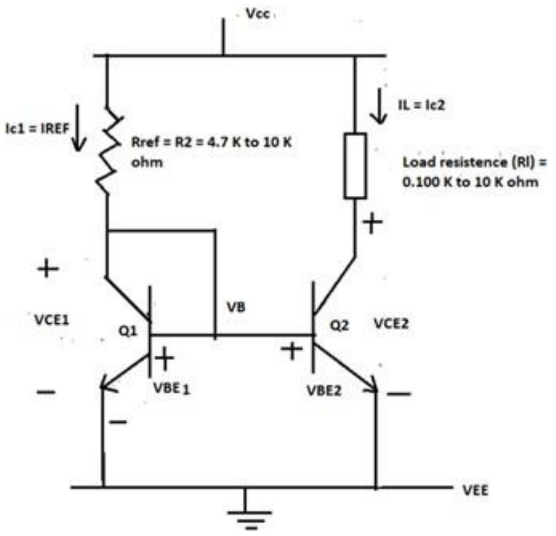


If a voltage is applied to the BJT, the base-emitter junction acts as an input quantity and the collector current is taken as an output quantity. The transistor acts as exponential voltage-to-current converter and by applying a negative feedback (simply by joining the base and the collector), the transistor can be reversed. The simplest bipolar current mirror implements this idea. It consists of two cascaded transistor stages acting accordingly as reversed and direct voltage-to-current converters. The emitter of Q_1 is connected to ground and the collector-base voltage is zero and the voltage drop across Q_1 is V_{BE}. If Q_1 and Q_2 are matched, that is if they have same device properties and if the mirror output voltage is chosen so the collector-base voltage of Q_2 is also zero, then the value of V_{BE} value set by Q_1 results in an emitter current matched in Q_2. Because Q_1 and Q_2 are matched, their β values also agree, making the mirror output current the same as the collector current of Q_1.

The main specifications that characterize a current mirror circuit are:

1. Current transfer ratio
2. AC output resistance
3. Voltage drop

CIRCUIT DIAGRAM:



Current mirror circuit

PROCEDURE:

1. Make the connections as given in the circuit above.
2. I_{REF} is generated with respect to $R_2 = R_{REF}$ = 4.7 K Ω, V_{cc} = 12 volt.
3. I_{C2} (collector current of Q_2) was observed.
4. Load resistance, R_l is varied and the corresponding collector current is noted down.
5. Repeat the procedure 1 to 4 for R2 = R_{REF} = 10 K Ω, Vcc = 12 volt.
6. The value of Load resistance (R_l) for which $I_{c1} = I_{c2}$, the circuit can be designed which acts as current mirror circuit.

OBSERVATION TABLE:

$R_{ref} = R_2$ = 4.7 kΩ			$R_{ref} = R_2$ = 10 kΩ		
Load resistance(R_l)	Ic1(mA)	Ic2(mA)	Load resistance(R_l)	Ic1(mA)	Ic2(mA)
100 Ω			100 Ω		
200 Ω			200 Ω		
400 Ω			400 Ω		
600 Ω			600 Ω		
800 Ω			800 Ω		
1k Ω			1k Ω		
2k Ω			2k Ω		

3k Ω			3k Ω		
4k Ω			4k Ω		
5k Ω			5k Ω		
6k Ω			6k Ω		
7k Ω			7k Ω		
8k Ω			8k Ω		
9k Ω			9k Ω		
10k Ω			10k Ω		

CONCLUSION:

The collector current I_{c2} was found approximately equal to the collector current I_{c1} at a particular value of R_l. It was verified for two different value of $R_2 = R_{REF}$=4.7 kΩ and 10 kΩ.

PRECAUTIONS:

1. Ensure that the polarity of the power supply is properly connected.
2. There should be no loose contacts at the junctions.

TYPICAL QUESTIONS:

1. What is a current mirror in BJT?
2. How do you construct a current mirror using a BJT and MOSFET?
3. What is current sinking and current sourcing?
4. What are the applications of current mirror circuit?
5. What are the different techniques of designing current mirror circuits?
6. What is the difference between a practical and an ideal current mirror circuit?
7. What are the specifications of a proper current mirror circuit?
8. What are the limitations in real current mirror circuits?

OTHER RELATED CURRENT MIRROR CIRCUIT DESIGNS:

1. Wilson current mirror
2. Widlar current mirror
3. Buffered feedback current mirror
4. Cascaded current mirror

EXPERIMENT – 10

DESIGN AND STUDY OF INPUT (DIFFERENTIAL PAIR) AND OUTPUT (DARLINGTON) STAGE OF OPAMP.

OBJECTIVE:

To conduct experiment to study the differential pair amplifier connected at input side and Darlington stage at output side of internal structure of OPAMP.

APPARATUS AND COMPONENTS REQUIRED:

1. Bread Board
2. Regulated power supply
3. Digital storage oscilloscope
4. Function generator
5. NPN Transistor BC547A & BC107BP
6. Resistor (4.7KΩ, 10 KΩ, 1MΩ, 100KΩ)
7. Capacitor (two 10μF)
8. Connecting wires
9. Multimeter

THEORY AND EXPLANATION:

The internal structure of OPAMP is shown in figure 1.

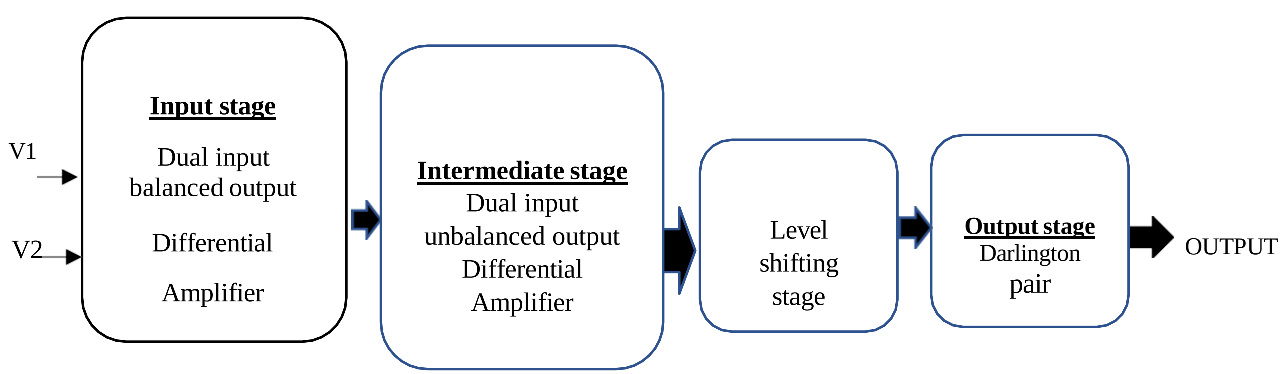


Fig.10.1 Block diagram of internal structure of OPAMP.

1. **Differential Amplifier**

A differential amplifier is most widely used circuit building block in analog integrated circuit. For instance, input stage of every op-amp amplifier is a differential amplifier. BJT differential amplifier is the basis of a very high-speed logic circuit family called emitter-coupled logic (ECL). The differential amplifier as the name suggests amplifies the difference between two input signal vin1 and vin2. BJT differential pair configuration consists of two matched transistors Q1 and Q2, whose emitters are formed together and biased by a constant current source I. Latter is usually implemented by a transistor circuit. The two collectors may be connected to another transistor rather than to resistive loads. It is essential though that the collector circuits be such that Q1 and Q2 can never enter saturation.

Gain of differential amplifier is given by:

$$A_d = \frac{V_0}{V_d}$$

$$where, V_d = V_{in1} - V_{in2}$$

CIRCUIT DIAGRAM:

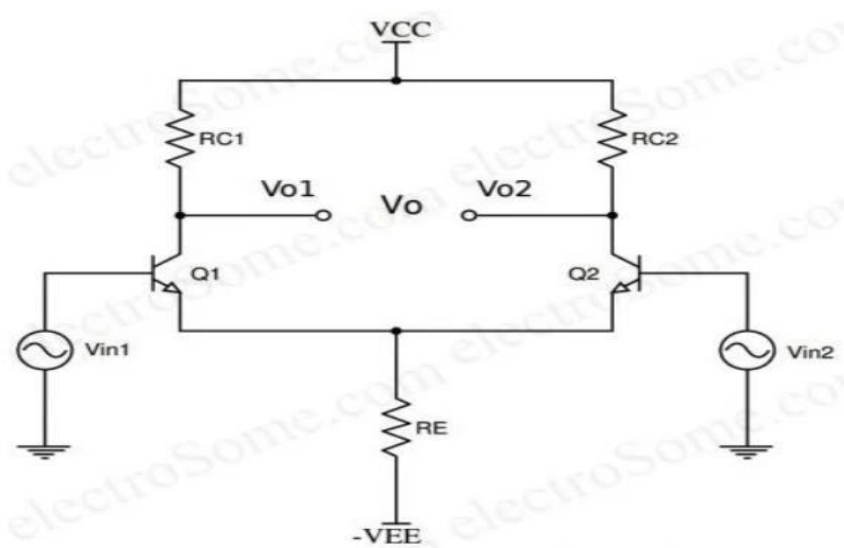


Fig.10.2 Differential amplifier using transistor where (R_{C1}=R_{C2}=4.7KΩ & R_E=10KΩ, V_{CC}=12V and V_{EE}=-12V)

PROCEDURE:

1. Connect the circuit as per diagram on the bread-board.
2. Connect 12V power supply.
3. Connect the vin1 and vin2 voltages to the circuit.

4. Measure the output voltage from oscilloscope.
5. Find the gain using output voltage and difference of input voltage.

OBSERVATION:

SL. No.	Vin1	Vin2	Vout	Ad (Gain)
1.	10mV	20mV		
2.	20mV	5mV		
3.	5mV	8mV		

2. DARLINGTON PAIR

The Darlington transistor (often called a Darlington pair) is a compound structure consisting of two bipolar transistors (either integrated or separated devices) connected in such a way that the current amplified by the first transistor is amplified further by the second one. This configuration gives a much higher common/ emitter current gain than each transistor taken separately. In the Darlington pairs, transistor collectors are tied together and the emitter of the first is directly coupled to the base of the second transistor. The total gain, which is often 1000 or more, is the product of the gain of the individual transistors. For large currents it is standard and good procedure to use a Darlington pair of transistors, rather than a single one, which effectively acts like a single transistor with β that is the two βs of the individual transistors.

The Darlington pair has an overall current gain of:

$$\beta_d = \beta_1 \beta_2 \qquad (10.1)$$

$$where, \beta_d = \frac{I_C}{I_B}$$

The key advantage of the Darlington configuration is that the total current gain of the circuit equals the product of the current gain of two devices since its current gain is much higher. It combines two bipolar transistors in a single device; hence they require lesser space than configurations that use two discrete transistors. Darlington connection can have high input impedance and can produce very large outputs current. The disadvantage is the larger saturation voltage compared to single transistor configurations. Darlington transistors also have a higher base emitter voltage which is sum of both base emitter voltage.

CIRCUIT DIAGRAM:

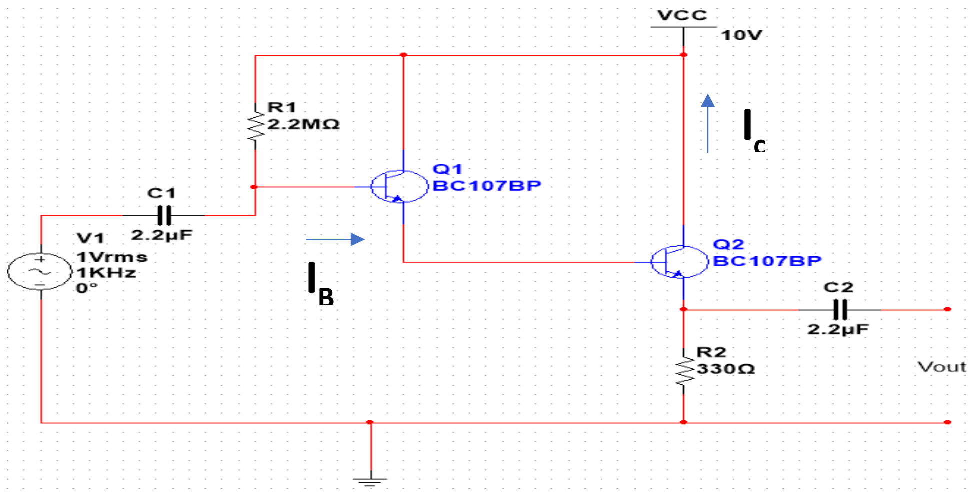


Fig. 10.2: Circuit diagram of Darlington pair.

PROCEDURE:

1. Connect the circuit as shown in the figure 2.
2. Note down input current I_B and output current I_C for different value of source voltage.
3. Check β1, β2 and the overall current gain relationship for Darlington pair (βd = β1β2) is valid for different value of source voltage.

OBSERVATION:

SL. No.	V1	β1	β2	βd
1.	1V			
2.	2V			
3.	5V			

PRECAUTIONS:

1. The breadboard should be handled carefully.
2. All connections should be neat and tight.